Introduction

The purpose of this application note is to provide a generic procedure for tuning the matching networks required for the F1478 amplifier. A series of specific steps are recommended to optimize device performance in the band of interest. It is suggested that small-signal parameters such as gain peak (S21) and return loss (S11, S22) are tuned first. Post small-signal tuning should then be followed by linearity (OIP3, OP1dB) performance tuning. Finally, it is highly recommended that stability be evaluated, especially at high frequencies above 10GHz. Figure 2 shows the F1478 application circuit. Figure 3 shows the F1478 pin assignments and Table 1 summarizes the different tuning networks contained in the reference circuit shown in Figure 1 and how tuning these networks impact the overall device performance.

Figure 1. F1478 Block Diagram and Tuning Areas

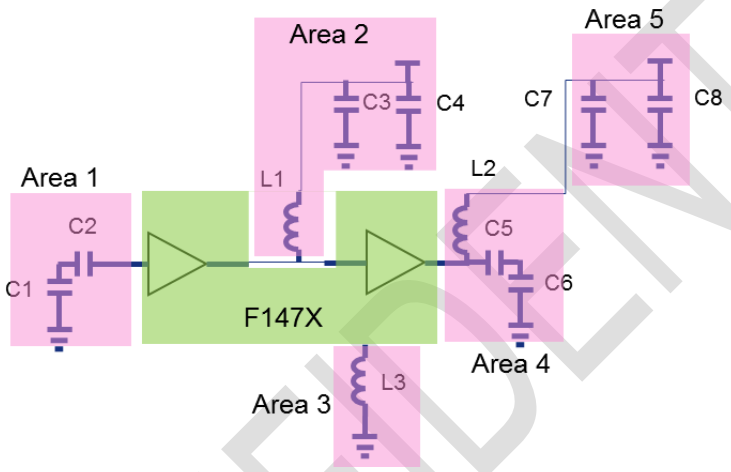


Table 1. Parameter vs. Tuning Trade-off Space

Parameter	Area that influences	Comments
Input return loss (S11)	1 (Major), 2(Minor)	Area 2 also affects the gain peak frequency. See section 1.3.1 Inter-stage Match Example on page 6 for additional information
Output return loss (S22)	4 (Major), 2(Minor)	Area 2 also affects the gain peak frequency. See section 1.3.1 Inter-stage Match Example on page 6 for additional information
Gain peak	Area 2	Larger L1, gain peak will be at lower frequency. Below 4GHz band, only tune the L1, when frequency goes higher, tune C3 and C4 as well
Linearity	4, 3	Larger L3 improves linearity at lower frequency. Area 4 – See to section 1.4 Linearity on page 8 for additional information.
Stability	1, 2	See section 2 Stability on page 10 for additional information.
Gain flatness	4, 1	Gain flatness is improved by slightly tuning return loss.

Figure 2. F1478 Application Circuit

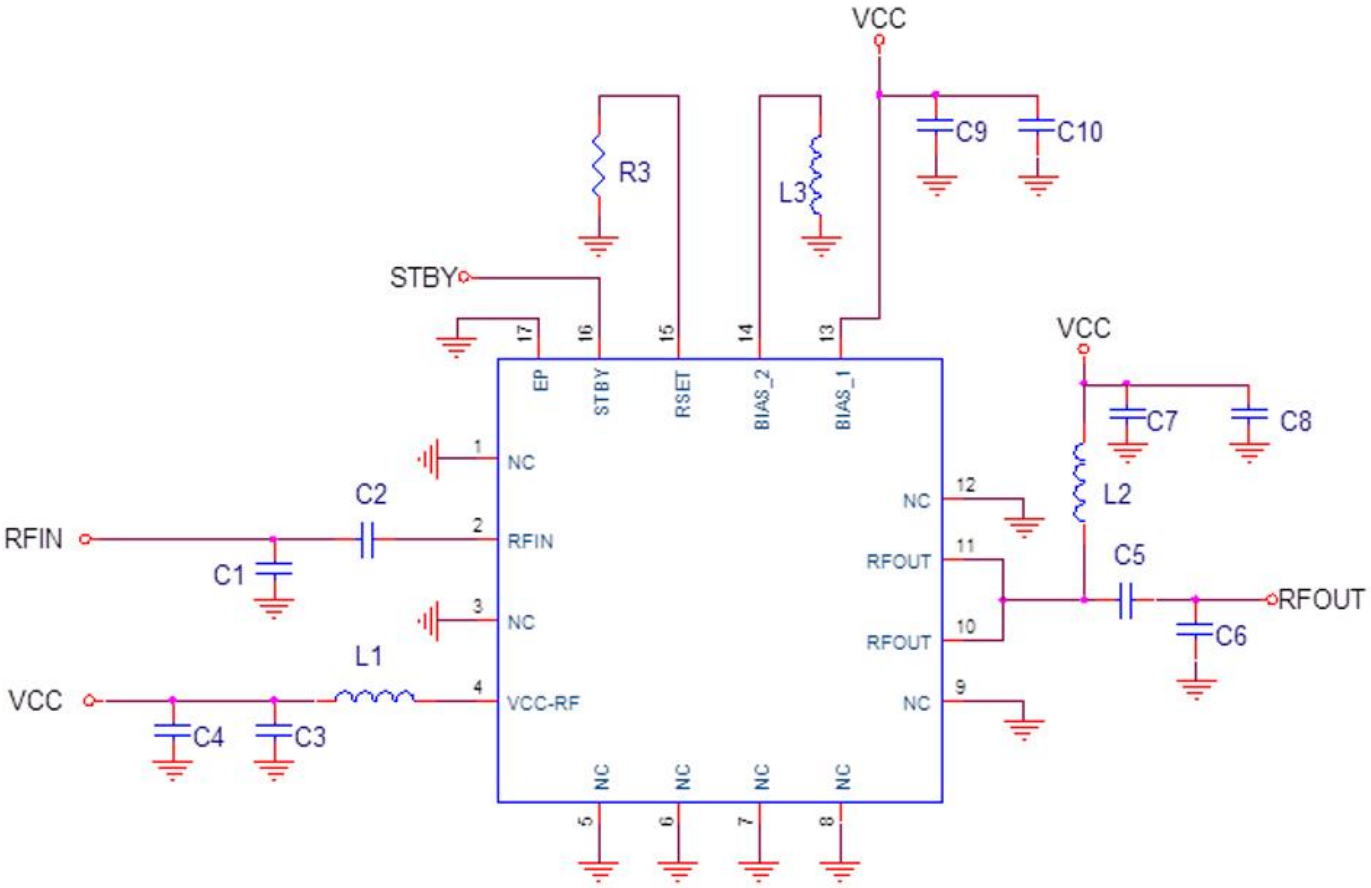
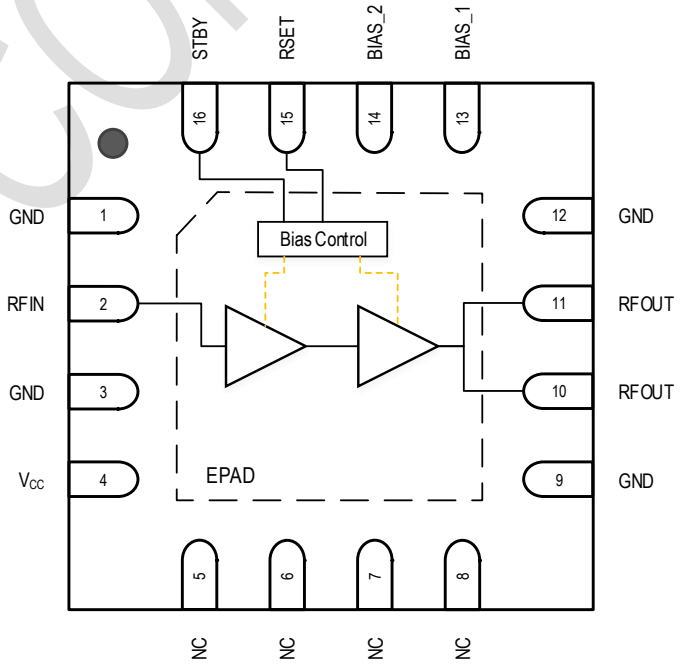


Figure 3. Pin Assignments for F1478 3 × 3 × 0.9 mm VFQFPN Package – Top View



1. Parameter Tuning

The following sections will describe recommended methods for F1478 tuning to optimize both small-signal, linearity, and if necessary, stability performance.

1.1 Gain Peak

Tuning elements L1, C3, and C4 together act as both a bias network and decoupling components for the first stage and an inter-stage matching network between the amplifier stages. Component value selection and placement is critical for S21 gain peak and for overall device stability. Components C3 and C4 function as both supply decoupling capacitors and as matching elements for the inter-stage network, forming shunt elements to ground after the series L1. In certain cases, C3 has been shown to affect gain peak (and stability) as well.

A larger inductance value for L1 results in gain peak at lower frequencies.

1.2 Inter-stage Component Selection – Gain Notch Avoidance

The following is a hypothetical example of using poorly chosen decoupling components used in the inter-stage matching network without first simulating the in band interaction at RF frequencies. C4 is a standard choice for low frequency decoupling, with C3 being a standard choice for high frequency decoupling.

The data shows the effects of the chosen components in the inter-stage matching network. The F1478 was measured on a 3 port VNA and an S3P file was exported for use by ADS. Within ADS, the S3P file was connected to the inter-stage match components using the models provided by the manufacturer.

The parasitics of L1 (ESR of appx. 0.5 ohms) and C3 & C4 (ESR of 0.2 ohms, series inductance of 0.4nH) can introduce an undesired notch seen near the gain peak frequency.

Figure 2 shows the measured S21 forward gain response when using the components models and values specified in Table 2 for L1, C3, and C4. Note the notch in S21 forward gain response at approximately 2.4GHz. This notch is due to the inter-stage matching network response formed by component parasitics at that frequency.

Figure 5 shows the impedance the network using component values specified in Table 2 for L1, C3, and C4.

Figure 6 shows the return loss of the first stage bias network and inter-stage matching network.

Table 2. Inter-stage Match Component Values

Component Reference	Manufacturer	Reference Part Number	Component Value
C3	Murata	GRM1555C2A5R0WA01	5pF
C4	Murata	GRM155R61H104KE104	100nF
L1	Murata	LQP15MN3N0B02	3nH

Figure 4. S21 Frequency Response of First Stage Bias Network and Inter-stage Match

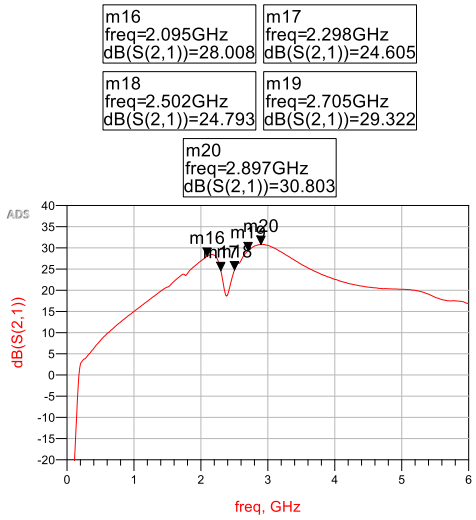


Figure 5. Impedance Plot of First Stage Bias Network and Inter-stage Match

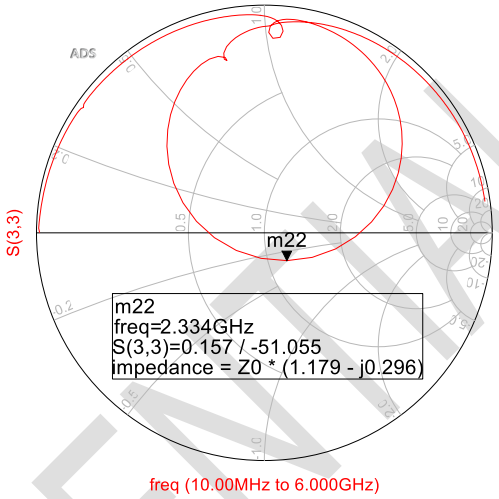


Figure 6. Return Loss Plot of First Stage Bias Network and Inter-stage Match

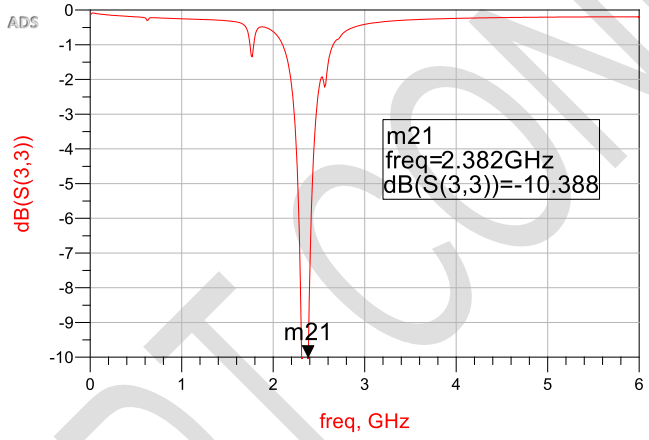


Figure 7 shows the IDT equivalent circuit model of the first stage bias network and inter-stage matching network with components referenced by Table 2. Instead of using the component models provided by the manufacturer in the previous figures, this equivalent circuit model is used for components and is connected to the S3P file in ADS.

Figure 8 shows the impedance of the first stage bias network and inter-stage matching network.
Figure 9 shows the return loss of first stage bias network and inter-stage match.
Note the notch in the impedance and return loss at approximately 2.55GHz. This will cause gain variation when connected to the F1478.

Figure 7. Evaluation Board Equivalent Circuit used for First Stage Bias Network and Inter-stage Match

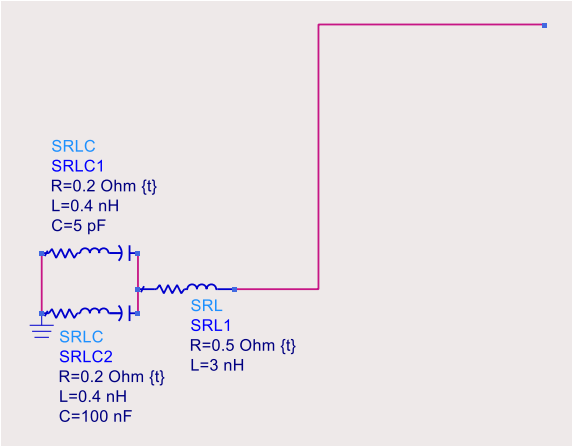


Figure 8. Impedance Plot of First Stage Bias Network and Inter-stage Match

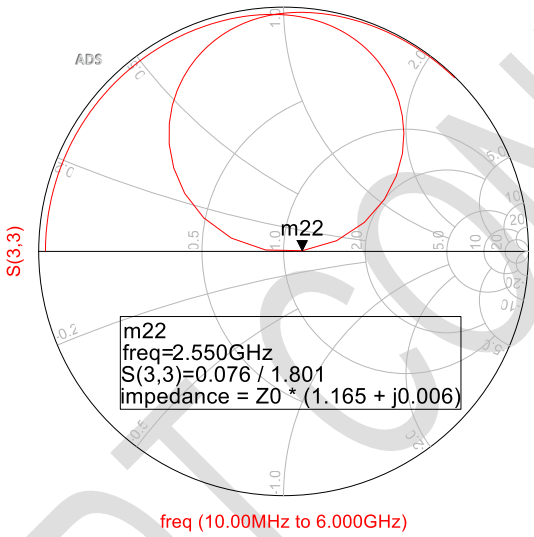
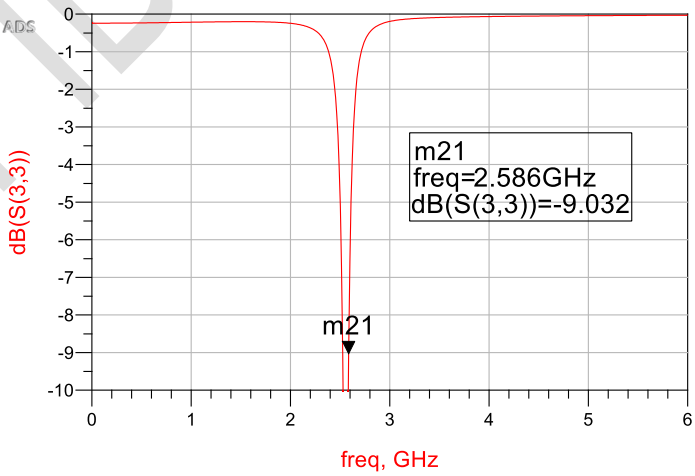


Figure 9. Return Loss Plot of First Stage Bias Network and Inter-stage Match



It is highly recommended that the designer simulate the impedance presented at Pin 4 of the F1478 to verify there is no component interaction or notch present within the band of operation.

1.3 Gain Peak Tuning Example

The following section presents information and a sample procedure for tuning the gain peak and return loss on the F1478. The F1478 is a two stage device, with the inter-stage match affecting the performance the device can achieve. When changing the inter-stage match (refer to Figure 1 Area 2), both the input (S11) and output (S22) return loss will shift.

When tuning the input return loss (refer to Figure 1 Area 1), it has a very small effect on the output return loss (S22) as compared to a traditional single stage amplifier.

The recommended tuning sequence is:

- Inter-stage matching (gain peak)
- Input matching (input return loss)
- Output matching (output return loss and linearity performance)

1.3.1 Inter-stage Match Example

In this example, the matching process begins by starting off with mid-band (2.3–2.7GHz) matching networks installed. The inter-stage matching starting values for L1, C3, and C4 are 3nH, DNI, and 100nF respectively. Refer to Figure 10 for starting peak gain performance and Figure 12 for return loss performance.

This hypothetical tuning example targets a desired usable band from 2.8–3.2GHz, center frequency is 3GHz. Since the target frequency is higher than the current matching components have optimized, begin by decreasing the inductance of L1 (recall that a higher inductance reduces the frequency of peak gain). By reducing the value of L1 to 1.6nH, the gain peak shifts to 3GHz, which is the center of the desired band. Refer to Figure 11.

Figure 10. S21 Inter-stage Match with L1 = 3.0nH

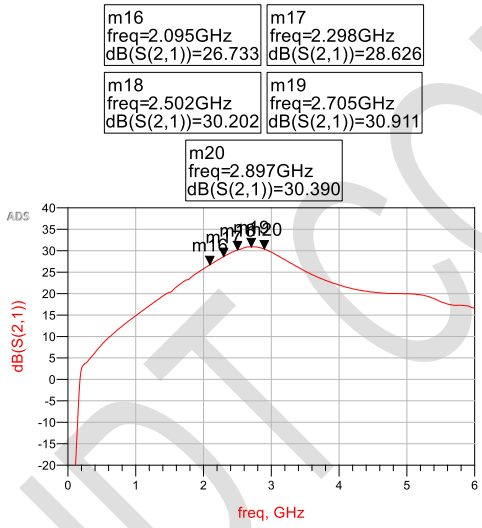
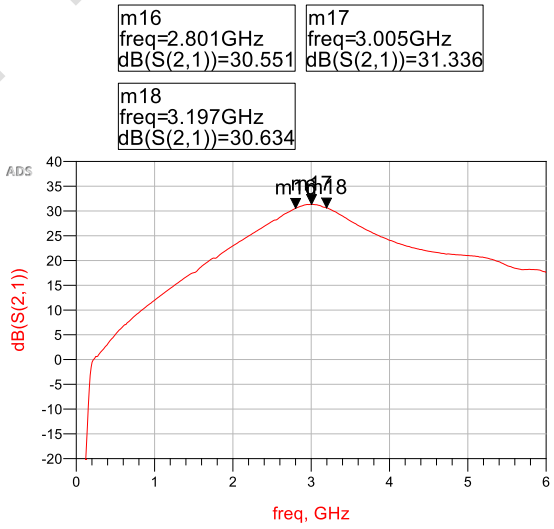


Figure 11. S21 Inter-stage Match with L1 = 1.6nH



1.3.2 Input Stage Match Example

Recall that input and output return loss will shift when changing the inter-stage match. In this case, the existing input match results are acceptable after the shift. After updating the L3 inductor to 1.6nH, the input return loss (S11) is shifted from approximately 2.9GHz (refer to Figure 12) to approximately 3.1GHz (refer to Figure 13). With additional work the match may be improved further.

Figure 12. S11 and S22 Input Match with L1 = 3.0nH

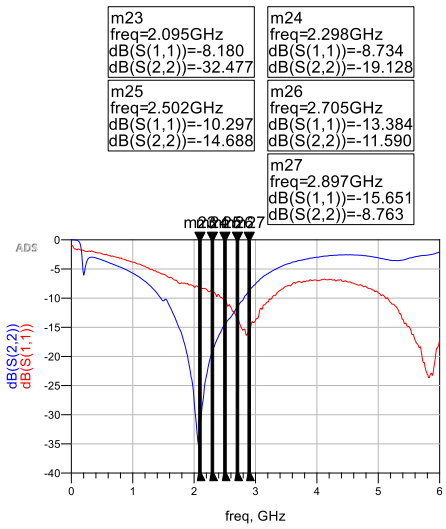
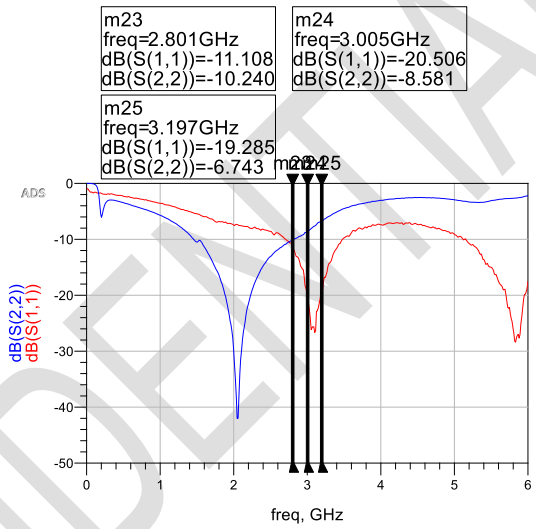


Figure 13. S11 and 22 Input Match with L3 = 1.6nH



1.3.3 Output Stage Match Example

The output return loss also shifts when changing the inter-stage match. However, in this case the output return loss is not acceptable, with the match centered too low in frequency around 2.1GHz, and the upper end of the band of interest has return losses greater than 10dB. Refer to Figure 14.

Changing the output match component values for C1 to 0.6pF, and C6 to 0.7pF yields an output return loss of approximately 20dB in the band of interest. Refer to Figure 15. In this example, a C6 = 0.7pF capacitor is chosen even though the output return loss minimum is not aligned with the center of the band of interest. With the F1478, a 1.5pF to 0.2pF capacitor at the output is needed for best linearity performance. This example highlights how the output match also plays a significant role in linearity performance in addition to return loss.

Figure 14. S21 Output Match with L1 = 3.0nH C1 = 0.5pF C6 = 1.2pF

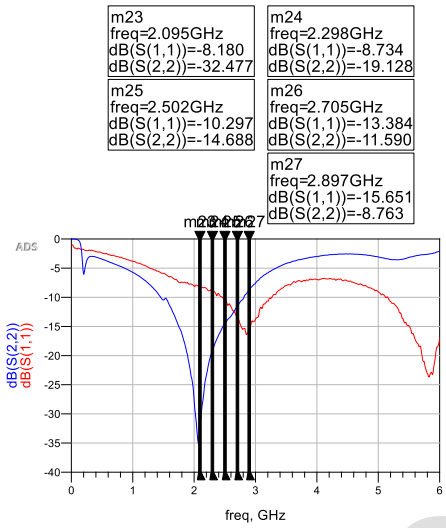
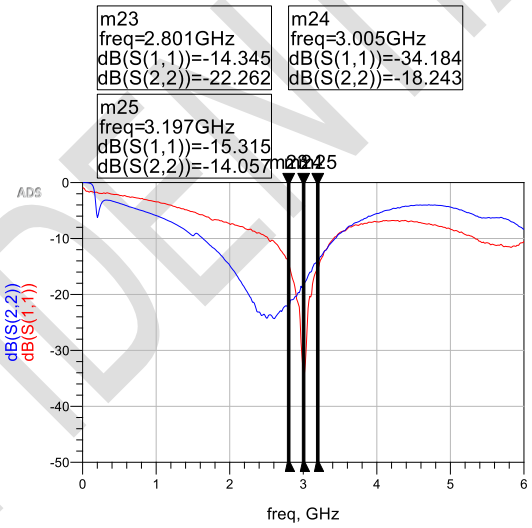


Figure 15. Output Match with L1 = 1.6nH C1 = 0.6pF C6 = 0.7pF



1.4 Linearity

As previously mentioned in the Parameter Tuning section, device output matching is not only for tuning the output return loss, but also the linearity performance. It is important to realize that tradeoffs can be made when tuning the output match, and not to focus solely on return loss when tuning the output match. The component L3 affects the linearity performance.

Typical values for L3 can be:

- 5–6GHz: L3 = 1.5nH
- 4–5GHz: L3 = 2.2nH
- 1–3GHz: L3 = 50ohm or larger inductor

  Note: Higher shunt resistance here results in higher IDDQ

Figure 16 shows a load pull contour of OIP3 at 2.5GHz. Red dots indicate higher OIP3, blue dots indicate lower OIP3. Presenting an impedance outside of the area swept results in poor output return loss (worse than 9dB).

Figure 17 shows a load pull contour of OP1dB. Red dots indicate higher OP1dB, blue dots mean lower OP1dB.

As shown below, the impedance for best OIP3 is not the best impedance for P1dB. These plots demonstrate the impedance presented to the device output will be a tradeoff between OIP3, P1dB, and output return loss. The decision on which to prioritize is left to the circuit designer.

Figure 16. OIP3 Load Pull Contour at 2.5GHz

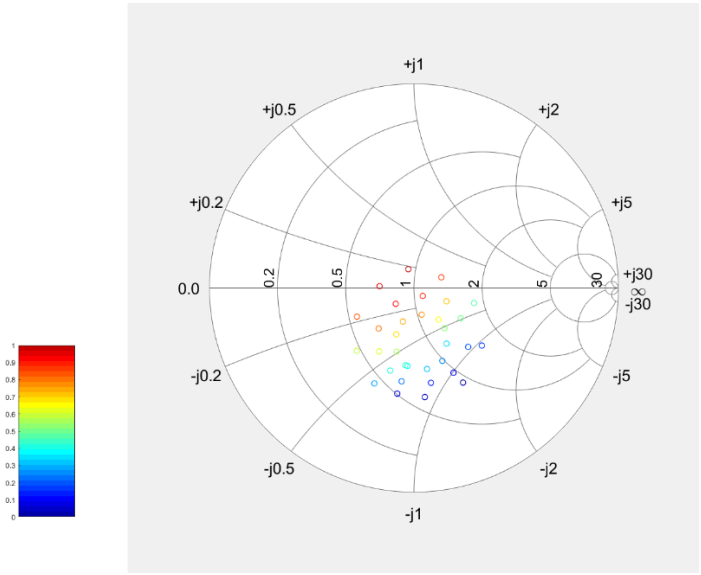


Figure 17. OP1dB Load Pull Contour at 2.5GHz

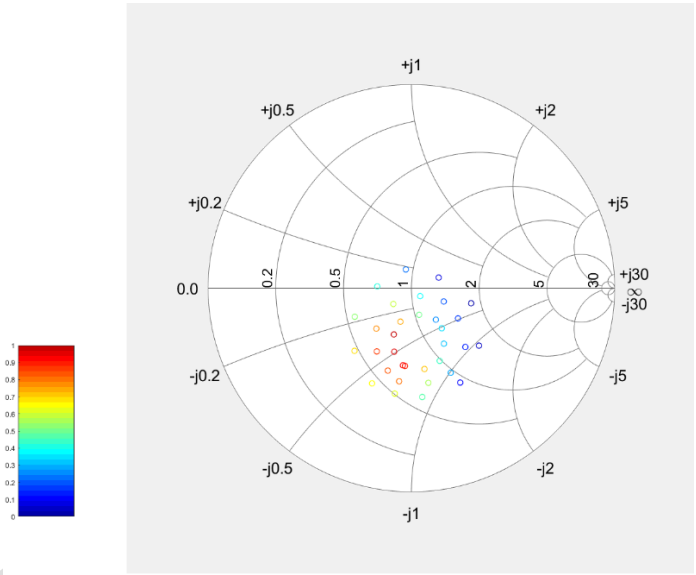
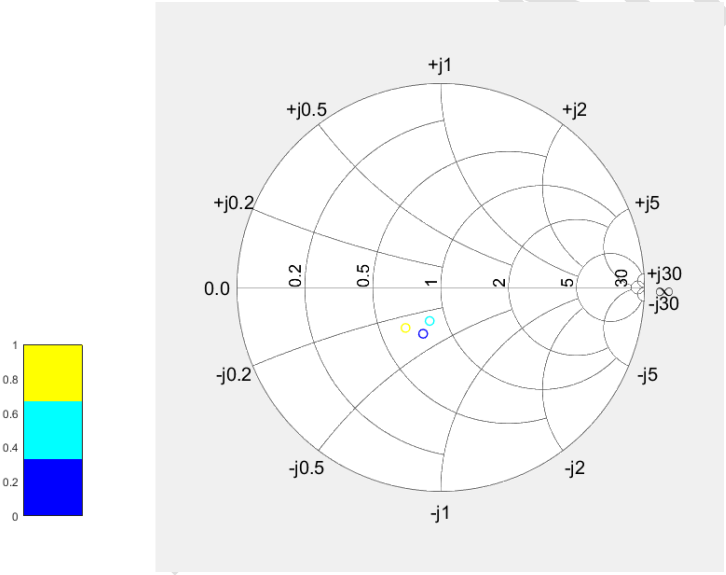


Figure 18 shows three recommended options for impedance to present to the device output in the 2.5GHz band. In this area of the Smith Chart, the device OIP3 performance is approximately 36dBm, OP1dB is approximately 24.5dBm, and output return loss (S22) is approximately 15dB (blue and cyan) and 10dB (yellow).

Figure 18. Optimum Impedance Locations at 2.5GHz



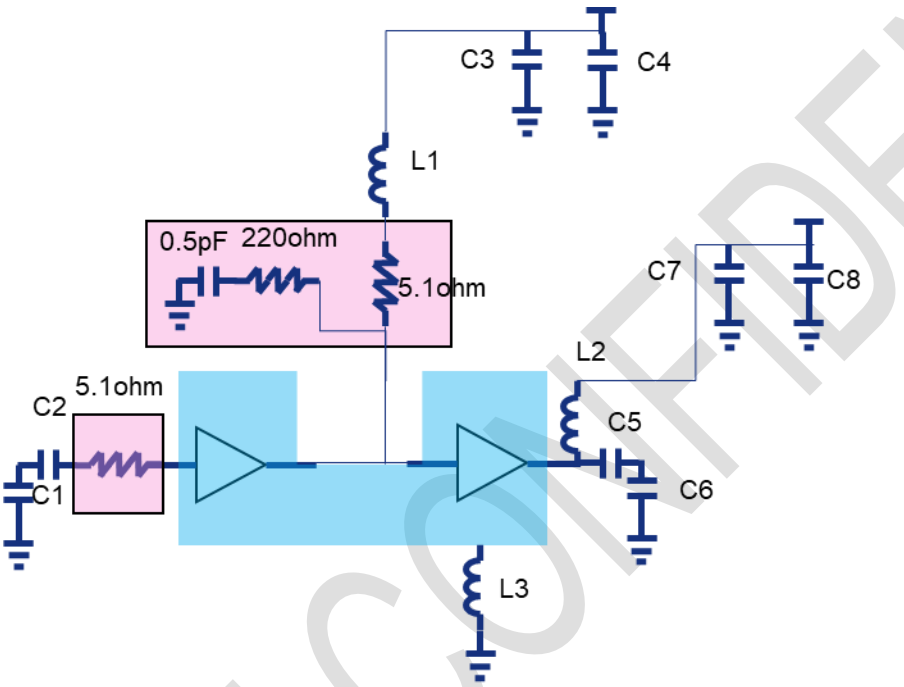
2. Stability

Benefits of two stage amplifiers include high gain and wide bandwidth. Encumbrances include multiple VCC pins and layout sensitivity, especially output to input coupling due to the increased gain which can cause feedback at high frequency and potential instability.

For the most robust design in terms of stability when implementing the F1478, it is recommended to add four additional components to the application circuit. They are shown in the pink boxes in Figure 19. They are damping networks designed to improve the stability of the part. As with any analog circuit, the values shows are only starting values and will require some tuning depending on the circuit layout implemented.

The values selected will be a tradeoff between performance and stability. The series resistor at the input will affect the amplifier noise figure, while the series resistor, shunt resistor, and shunt capacitor located between the inter-stage bias inductor and the VCC pin will affect gain and linearity.

Figure 19. F1478 Application Circuit including Damping Components



3. Layout

PCB layout is critical to achieving the specified performance of the F1478 High Gain RF Amplifier. This section will cover multiple topics the designer must consider when designing the PCB for the F1478. These topics will reinforce basic RF layout techniques as well as certain topics specific to the F1478 with the goal of achieving a successful layout that meets the requirements of the design.

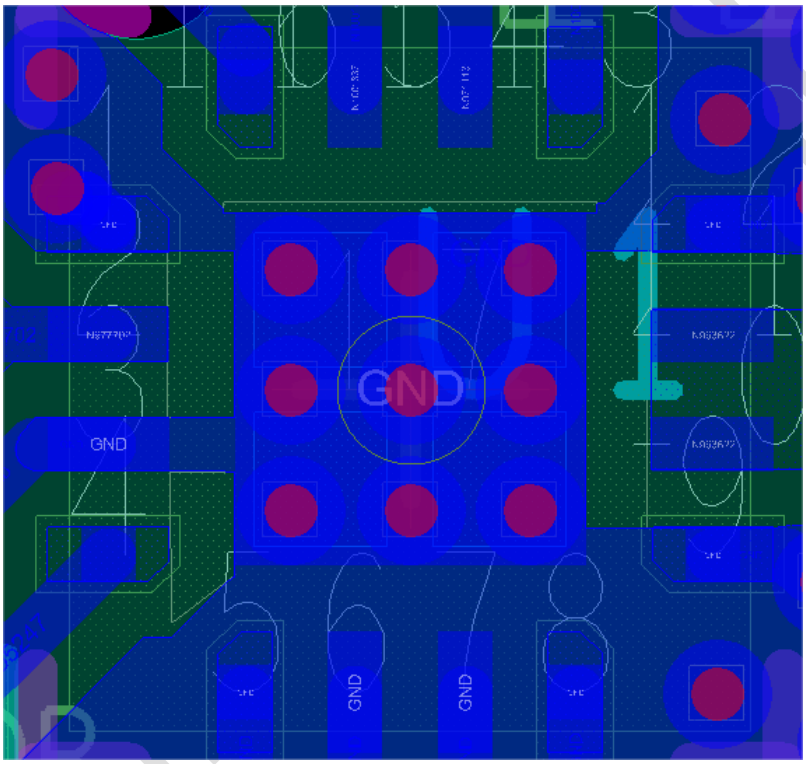
3.1 Grounding

The critical grounding point on the F1478 is the exposed paddle. It is recommended that at least QTY 9 vias with a drill size of 10 mil and 20 mil pad be placed under the device on the top layer. If the board fabrication technology used permits, it is preferred to increase the number of vias with smaller diameter. These vias are critical for both grounding and thermal performance.

The ground paddle should also be connected to the eight other pins on the top layer as well as connected to other ground planes adjacent to the bottom and corners of the device on the top layer. Place additional ground vias around the part where possible. Figure 20 shows additional recommended ground vias:

- As many ground vias that will fit under the package (minimum two recommended) between pins 1 and 16
- As many ground vias that will fit under the package (minimum one recommended) between pins 12 and 13
- As many ground vias that will fit under package (minimum one recommended) between pins 8 and 9

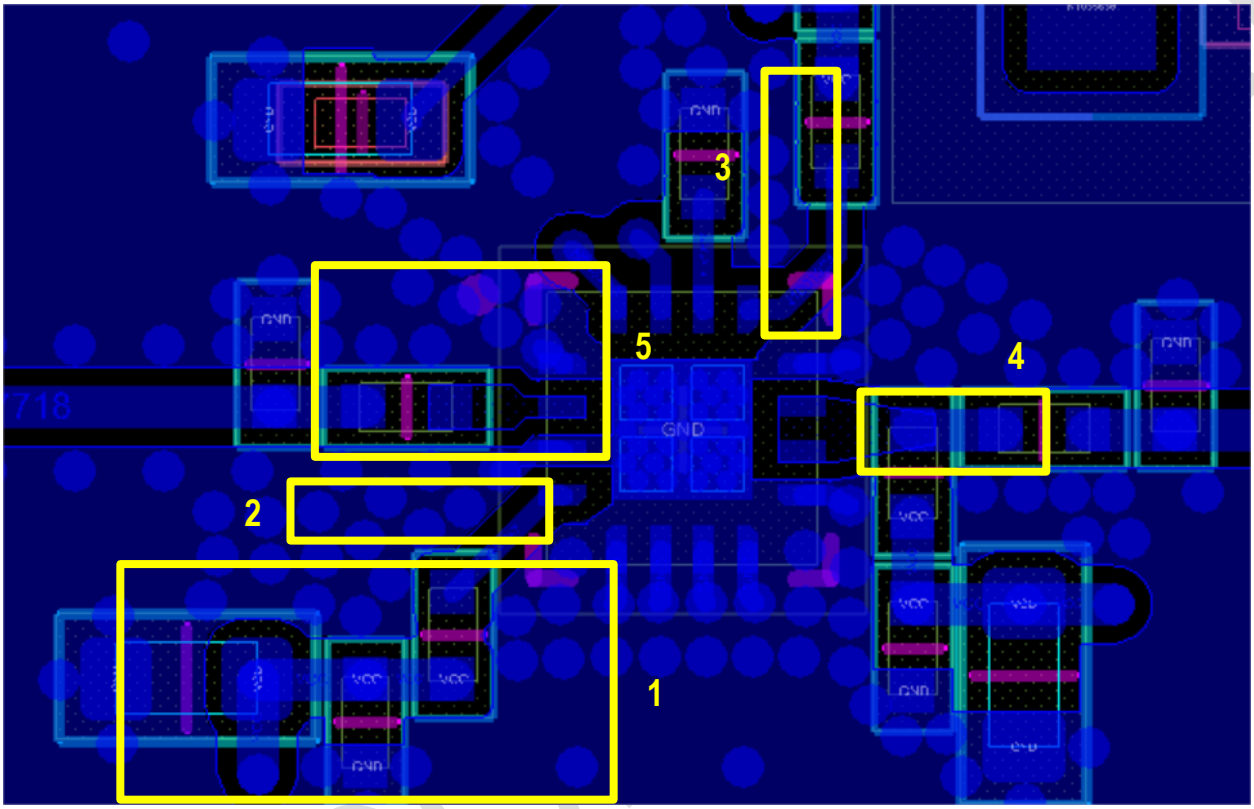
Figure 20. F1478 Recommended Ground Paddle via Placement



3.2 Component Placement

Component placement for the bias networks and matching components are critical to achieve specified performance. Figure 21 shows the location of components and their orientation to maximize the performance. Note all the components are on the top layer. Ground vias are used extensively in this design due to the high gain of this amplifier. Isolation of the RF input trace and associated matching network from the bias networks is critical. Isolation of the RF output pins to the bias networks must also be taken into consideration during layout.

Figure 21. F1478 Component Placement



Box 1 area of Figure 21: Place L1, C3, and C4 as close to IC as possible. It is recommended to treat pin 4 like an RF pin (without specifying a controlled impedance requirement). The placement of L1 on the top layer very close to the IC is critical, with the decoupling capacitors C3 and C4 also on the top layer as close to L1 as possible. This pin is RF sensitive, do not place any stub traces here. Use multiple grounding vias on C3 and C4 against the pad.

Box 2 area of Figure 21: Flood the top layer ground copper in this area to isolate pin 2 and pin 4. Note the number of vias used to connect the top layer of ground flood in this area. The ground island in this area also connects directly to pin 3 and continues to the paddle under the F1478.

Box 3 area of Figure 21: Place L3 as close to IC as possible on the top layer of the PCB (to minimize the parasitic inductance). Place ground vias around the entire perimeter of the ground side of L3 as shown in Figure 21.

Box 4 area of Figure 21: Do not route two thin separate traces from the dual RF output pins from pin 10 and pin 11. Use a use a single wider trace that tapers to the first connection to L2. L2 is placed closest to the IC. A short trace then runs to the matching network C5 / C6. Place at least 5 ground vias around the entire perimeter of the ground side of C6 as shown in Figure 21. Add ground vias along the perimeter of C5 as shown in Figure 21. Liberally place ground vias in the area between the RF output pins 10 &11 and pin 13 Bias_1 for isolation as shown in Figure 21.

Box 5 area of Figure 21: Place C1, C2 as close to the IC as possible on the top layer. Note the orientation of the series component as well as the shunt component. Place at least 5 ground vias around the entire perimeter of the ground side of C1 as shown in Figure 21. Add ground vias to isolate pin 2 from pin 4. Note the RF input trace in this layout is coplanar waveguide with annular ring of the ground vias against the edge of the ground flood spaced evenly.

4. Summary

The designer should simulate the impedance presented at Pin 4 of the F1478 to verify there is no component interaction or notch present within the band of operation.

When tuning the matching networks associated with the F1478, it's recommended that parameters are tuned in a certain order.

- Inter-stage matching (gain peak)
- Input matching (input return loss)
- Output matching (output return loss and linearity performance - OIP3 and OP1dB)
- Stability

Layout guidelines provided must be implemented to realize a stable amplifier that meets the specifications.

- Proper paddle grounding
- Component location
- Proper node isolation
- Component grounding
- Output trace recommendation

Revision History

Revision Date	Description of Change
August 7, 2019	Initial release.