

F5268/F5288

The F5268/F5288 Evaluation System (EVS) is designed to help you evaluate the F5268/F5288 Beamformer device. This document provides the information necessary to use the F5268/F5288 EVS and a brief overview of the associated control software Graphical User Interface (GUI). Renesas recommends that you review the F5268 and F5288 datasheets and use them as a reference to supplement the information provided in this document.

Features

- F5268: 24.25 to 27.5GHz operation
- F5288: 26.5 to 29.5GHz operation
- Four radiation elements per polarization channel (8 total)
- TX/RX operation (half duplex)
- 4-bit chip address (hard-wired/programmable)
- Integrated PTAT, PTAT², and Bandgap generator
- Internal temperature sensor and power detector
- Up to 95MHz SPI control
- Advanced SPI with 2048 programmable state memory
- Analog supply voltage: +2.4V to +2.6V (+2.5V nominal)
- Dedicated PA supply voltage: selectable between +2.4V to +2.6V and +3.0V to +3.3V

	Important Safety Warning: These procedures can result in high currents, which can cause severe injury or death and/or equipment damage. Only trained professional staff should connect external equipment and operate the software.
	Important Equipment Warning: Ensure the correct connection of all cables. Supplying the board using the wrong polarity could result in damage to the board and/or the equipment.

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1. F5268/F5288 Evaluation System Overview

1.1 Evaluation System Kit Contents

- F5268/F5288 Evaluation Board (EVB, see item 1 in Figure 1)
- FT2232HL Digital Interface Board (see item 2 in Figure 1)
- USB-to-Micro USB cable (see item 3 in Figure 1)

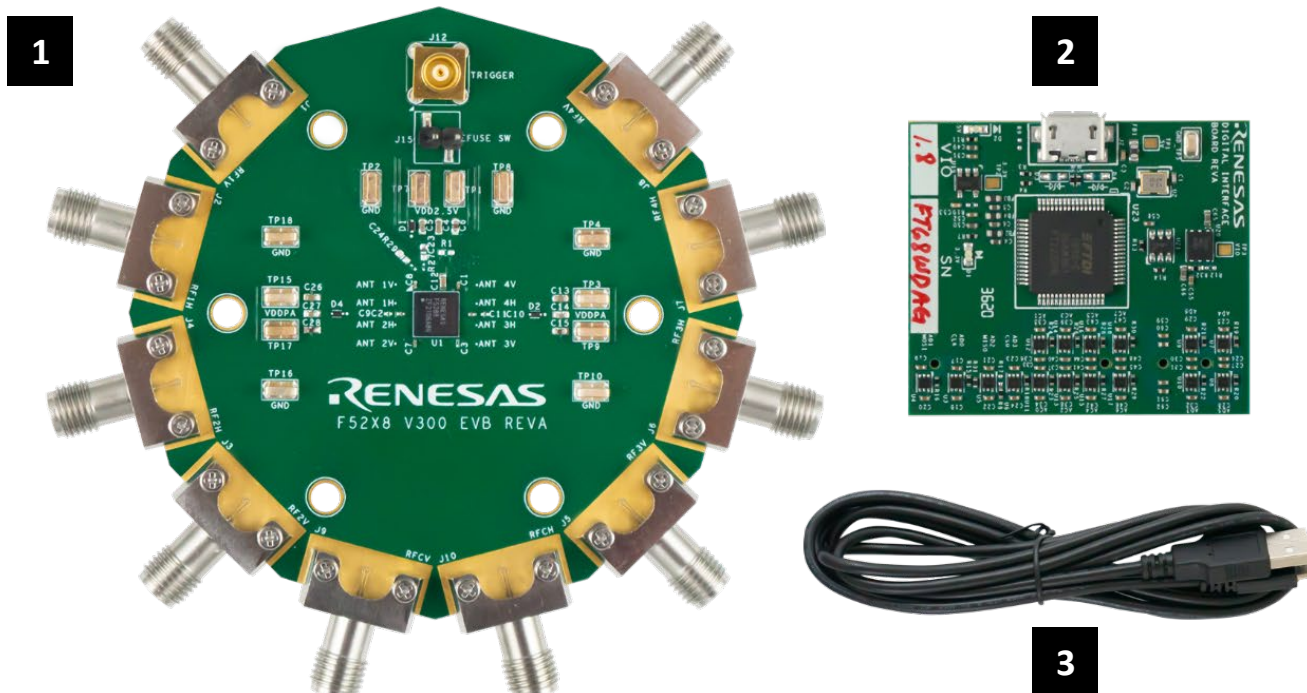


Figure 1. Kit Contents

1.2 Evaluation Board

Figure 2 identifies the location of the power supply, digital control headers, and RF I/O ports.

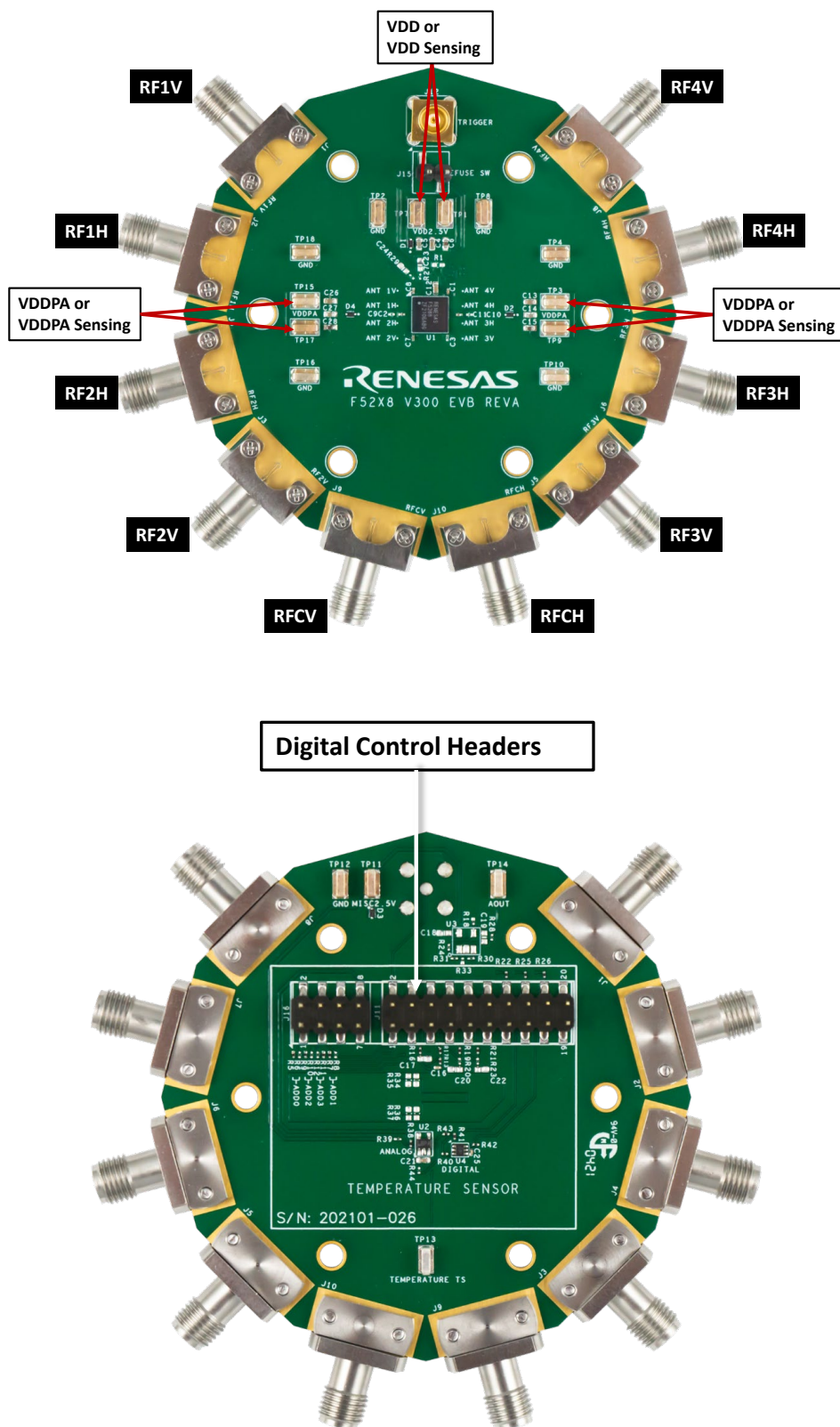


Figure 2. F5268/F5288 Evaluation Board – Top and Bottom

Table 1. Connector Descriptions

Connector	Description	
J1	RF1 vertical common port	
J2	RF1 horizontal channel port	
J3	RF2 vertical channel port	
J4	RF2 horizontal common port	
J5	RF3 vertical channel port	
J6	RF3 horizontal channel port	
J7	RF4 horizontal channel port	
J8	RF4 vertical channel port	
J9	RFC vertical channel port	
J10	RFC horizontal channel port	
J11	Digital control header (2×10) 1 – SDA_I2C 2 – Equip_Trigger 3 – SCL_I2C 4 – LNASW_MCU 5, 7 – No connection 6 – RESETB_MCU	8 – STRB_MCU 9, 10, 11, 13, 15, 17, 19, 20 – GND 12 – CSB_MCU 14 – MISO_MCU 16 – SCLK_MCU 18 – MOSI_MCU
J12	Trigger	
J16	Digital control header (2×4) 1 – ADD0_MCU 2 – ADD2_MCU 3 – ADD1_MCU	4 – ADD3_MCU 5, 6 – GND 7, 8 – MISC_1.8V

Table 2. Selector Descriptions

Selector Block	Description	Factory Setting
J15	VDD EFUSE jumper (add a jumper once the EFUSE is burnt) 1 – DVDD (from CREG pin, A8) 2 – VDD_EFUSE (from EFUSE/CREG pin, B8)	Not connected

Table 3. Test Point Descriptions

Test Point	Description
TP1	VDD_2.5V (external power supply for chip VDD and 4-wire sensing)
TP2, TP4, TP8, TP10, TP12, TP16, TP18	GND
TP3	VDDPA (external power supply for chip VDDPA and 4-wire sensing)
TP7	VDD_2.5V (external power supply for chip VDD and 4-wire sensing)
TP9	VDDPA (external power supply for chip VDDPA and 4-wire sensing)
TP11	MISC_2.5V (external power supply for AOUT buffer opamp)
TP13	Temperature sensor test point

Test Point	Description
TP14	AOUT buffer op-amp test point
TP15	VDDPA (external power supply for chip VDDPA and 4-wire sensing)
TP17	VDDPA (external power supply for chip VDDPA and 4-wire sensing)

1.3 THRU Reference Fixture

The THRU reference fixture (optional part of the Evaluation System) is used to generate test equipment de-embed files for removing the effects of the EVB RF traces and connectors. AFR (Automatic Fixture Removal) is a commercial product available from test and measurement suppliers to create the de-embed files (.s2p) using measurements from the THRU Reference Fixture traces (2x half-fixture lines). The THRU board is laid out symmetrically so that the AFR process can generate two half-fixture s-parameter files. S-parameter de-embed files are available from the Renesas Application Support or your local field engineer. For information on purchasing the THRU Reference Fixture board in order to create your own de-embed files, please contact the Renesas Sales department.

1.4 FT2232HL Digital Interface Board

The FT2232HL digital interface board connects your computer to the F5268/F5288 EVB through a USB-to-Micro USB cable. It is designed to directly attach to the back of the F5268/F5288 EVB, as displayed in the following figure.

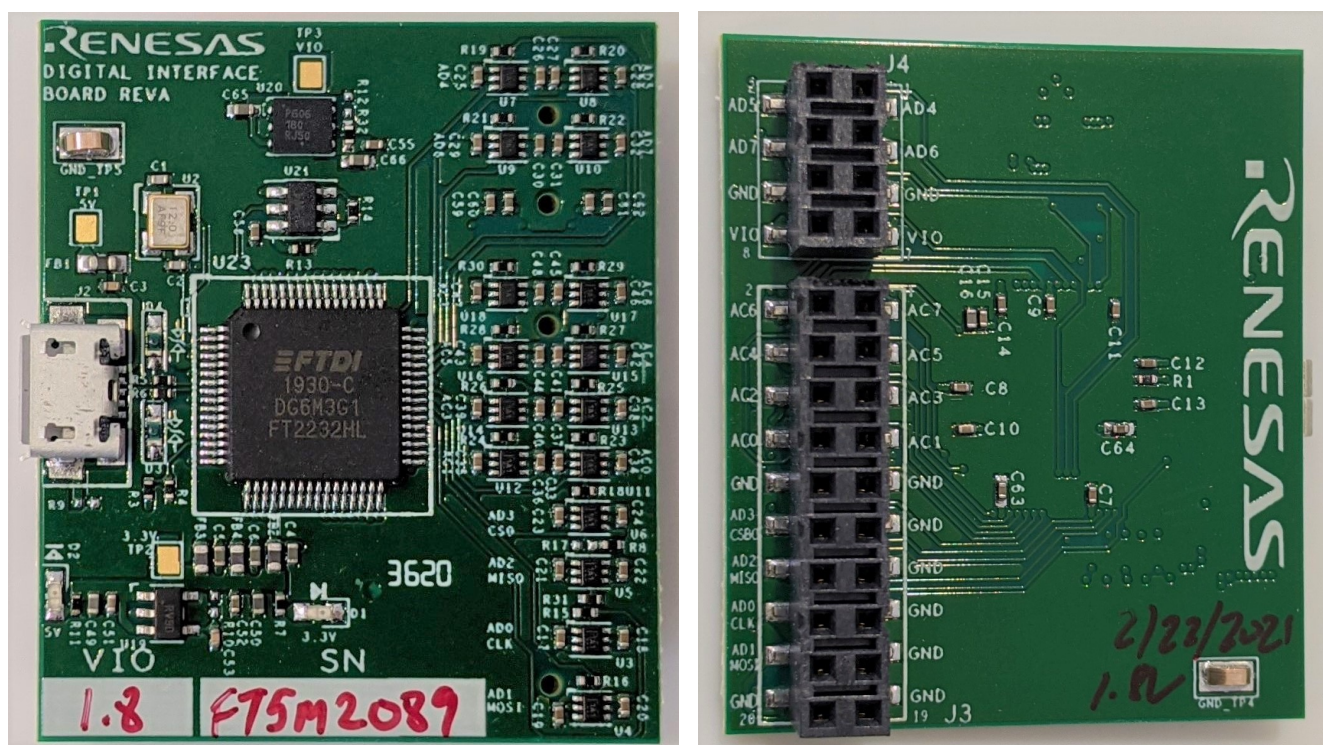


Figure 3. FT2232HL Digital Interface Board – Top and Bottom

2. Quick Start

2.1 Required or Recommended Test Equipment

- Power supplies with banana jack outputs capable of at least 2.5V and 2500mA rating.
- It is recommended to use a 4-wire remote sensing power supply for VDD and VDDPA when making any measurements for correlation with datasheet parameters. Removing all voltage drop introduced by the conductors and connectors is critical to achieving the datasheet specified performance. TP1 (+)/TP8 (-) and TP7 (+)/TP2 (-) on the EVB are provided to make connections as part of a 4-wire VDD connection to the power supply with standard lab test clips. TP3 (+)/TP4 (-), TP9 (+)/TP10 (-), TP15 (+)/TP18 (-), and TP17 (+)/TP16 (-) on the EVB are also provided to make connections as part of a 4-wire VDDPA connection to the power supply with standard lab test clips (see Figure 2 or Figure 4).
- Vector network analyzer capable of measuring from 24GHz to 30GHz

2.2 Computer Requirements and Setup

2.2.1. Computer Requirements

- Renesas Tx/Rx Beamforming Evaluation System Software installed
- USB 2.0 or 3.0 Interface
- Windows XP SP3 or later
- Processor: Minimum 1GHz
- Memory: Minimum 512MB; recommended 1GB
- Available Hard Disk Space: Minimum 600MB (32-bit OS), 1.5GB (64-bit OS); recommended 1GB (32-bit OS), 2GB (64-bit OS)
- Internet access during installation if the .NET framework (4.6.1 or later) is not currently installed on the system

2.2.2. Software Installation and Setup

1. Renesas Tx/Rx Beamforming Evaluation System Software is available from the Renesas secure portal or your field engineer.
2. Launch the software installation application (setup.exe).
Note: Your account must have administrator privileges to complete the installation.
3. Follow the on-screen prompts to complete the installation.

2.3 EVS Hardware Setup

Connect the EVS as displayed in Figure 4 using power supply cables with test clips and the provided USB-to-Micro USB cable. The digital interface board is attached to the back of the F5268/F5288 EVB. The typical VDD and VDDPA power supplies are 2.5V. VDD and VDDPA power supplies can be combined to a single power supply if a higher PA supply voltage is not needed. For full recommended power supply operating voltages, see the specific device datasheet.

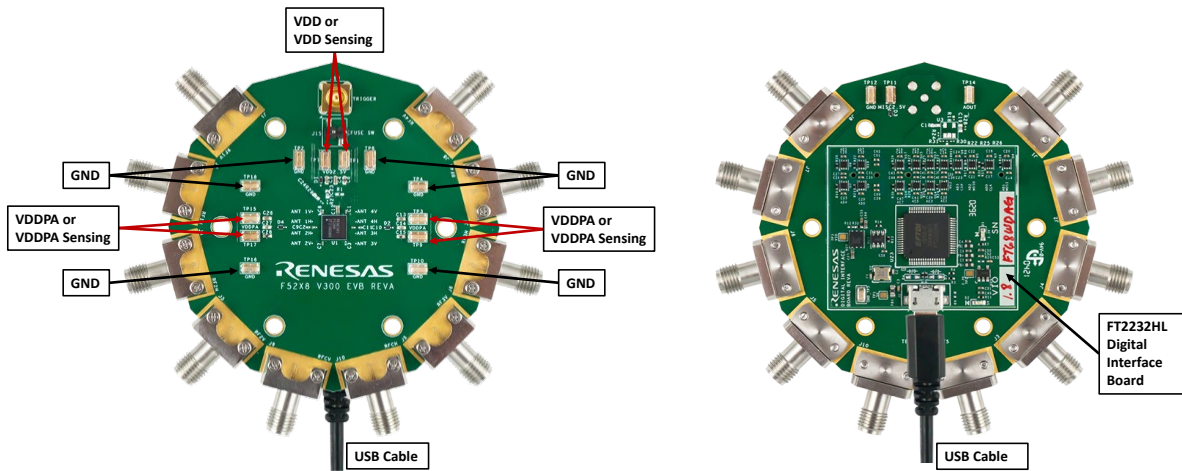


Figure 4. EVS Hardware Setup – Top and Bottom

2.4 Software Start-up

1. Open the application through the Windows Start menu or click on the application icon if saved on the desktop. The application appears as shown in Figure 5. The USB Interface Serial Number (item 1 in Figure 5) should be auto-detected if the FT232HL digital interface board is connected and recognized.
 - a. Select write speed, read speed, and chip address (see item 2 in Figure 5), then click **Detect** (see item 4 in Figure 5) to start the communication with the device.
 - b. Select the device from the **Device Selection** drop-down menu (see item 3 in Figure 5) if not properly auto-detected.

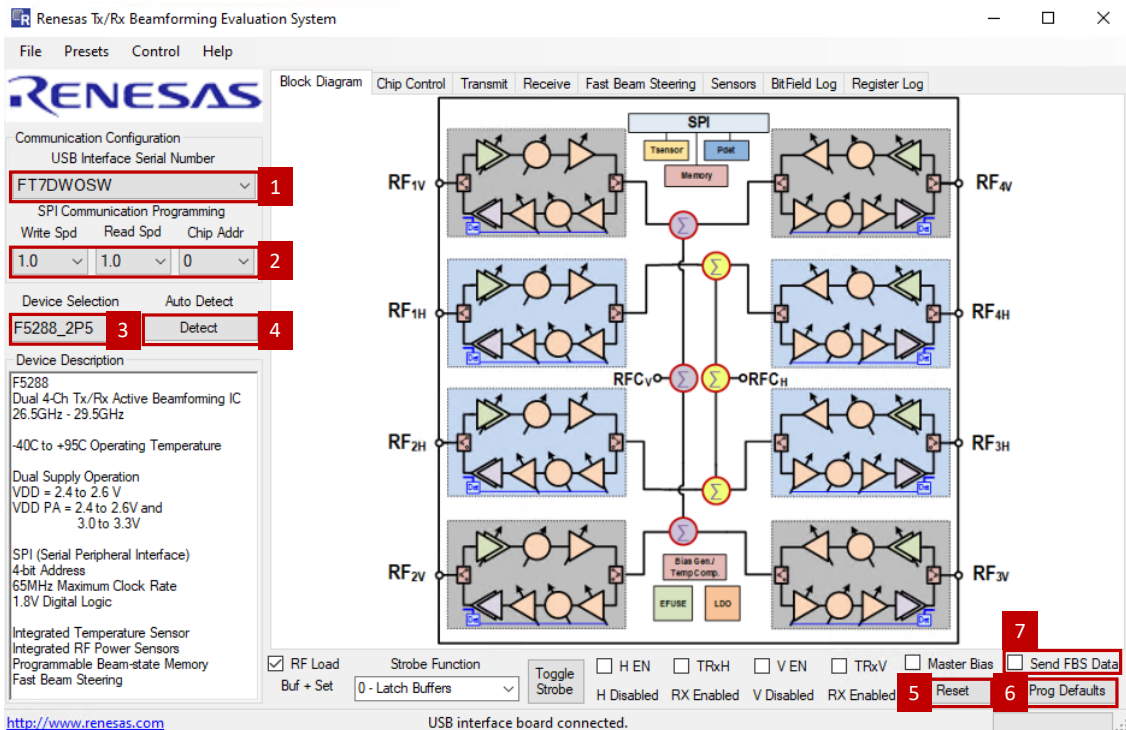


Figure 5. Application Control Panel at Start-up

2. The device can then be reset and programmed by clicking **Reset** button (see item 5 in Figure 5) and selecting **Yes** twice in sequence when prompted as shown in Figure 6. The **Reset** button will perform a hardware reset and ask whether the user would like to program the device with the recommended default

values. The GUI settings will be in sync with the hardware settings. Users can also program the device with the default recommended values at any given time by clicking **Prog Defaults** button (see item 6 in Figure 5).

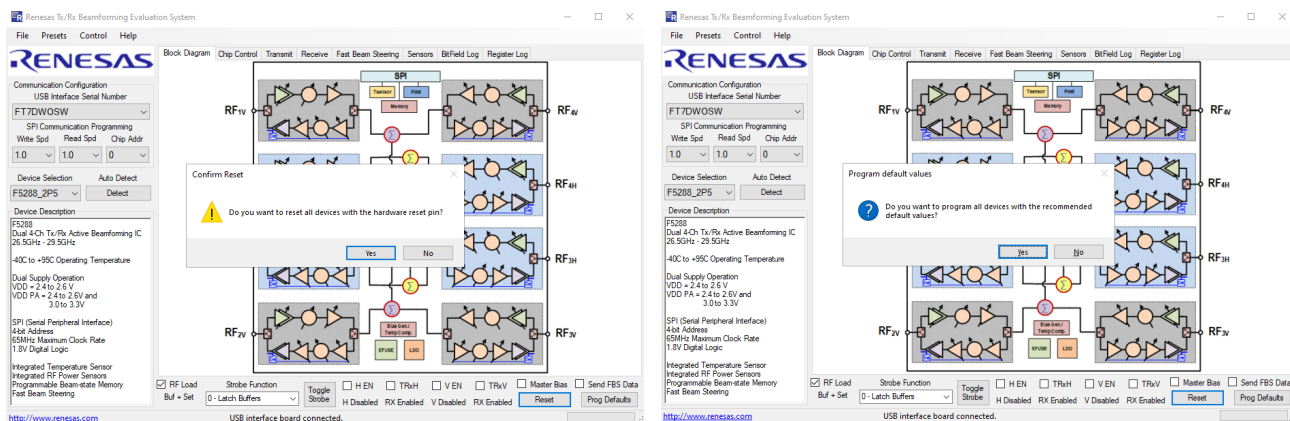


Figure 6. Toggle Reset Sequence

- To use the fast beam steering (FBS) lookup table (LUT) feature, the **Send FBS Data** checkbox (see item 7 in Figure 5) must also be selected before programming the device. An FBS LUT data can be loaded by selecting **Load Fast Beam Steering Lookup Table** in the File menu (see item 3 in Figure 7). A default FBS LUT file is provided with the EVS software as an example.

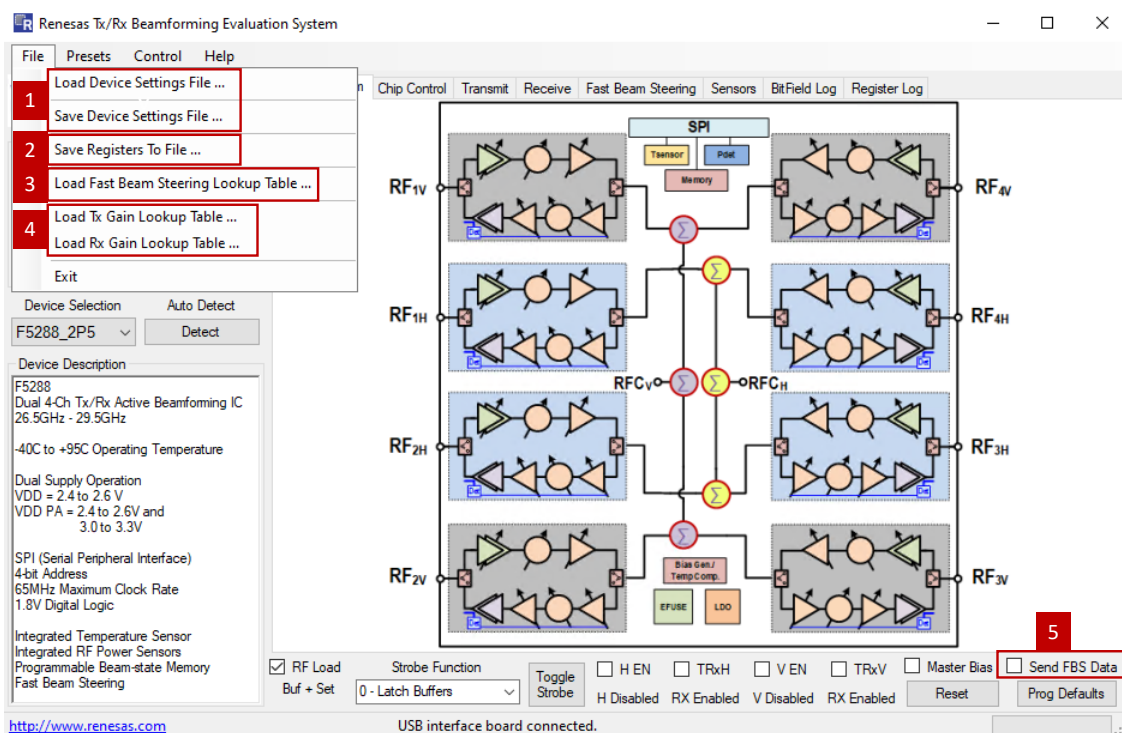


Figure 7. File Menu

- Device settings at any given time can be saved to an XML file and loaded back to the EVS software by selecting corresponding options in the File menu (see item 1 in Figure 7). Item 2 in Figure 7 will save all register offset addresses and values (in hexadecimal format) to a CSV file.
- For optimal RMS gain error, VGA gain attenuation for each TX/RX channel can be controlled using recommended LUTs, which will be automatically loaded by default when the device is programmed with recommended settings. Any modified TX/RX gain LUT can be loaded by selecting corresponding options in the File menu (see item 4 in Figure 7).

3. Software Functional Overview

Other control buttons that are also accessible on the main panel include the ability to program/toggle the Strobe pin (see item 1 and 2 in Figure 8), enable/disable H/V channels (see item 3 and 5 in Figure 8), and toggle between RX and TX for H and V channels (see item 4 and 6 in Figure 8). Specific register settings can be revised on different panels accessible using the panel tabs at the top (see item 7 in Figure 8). The block diagram tab only provides an overview of the system.

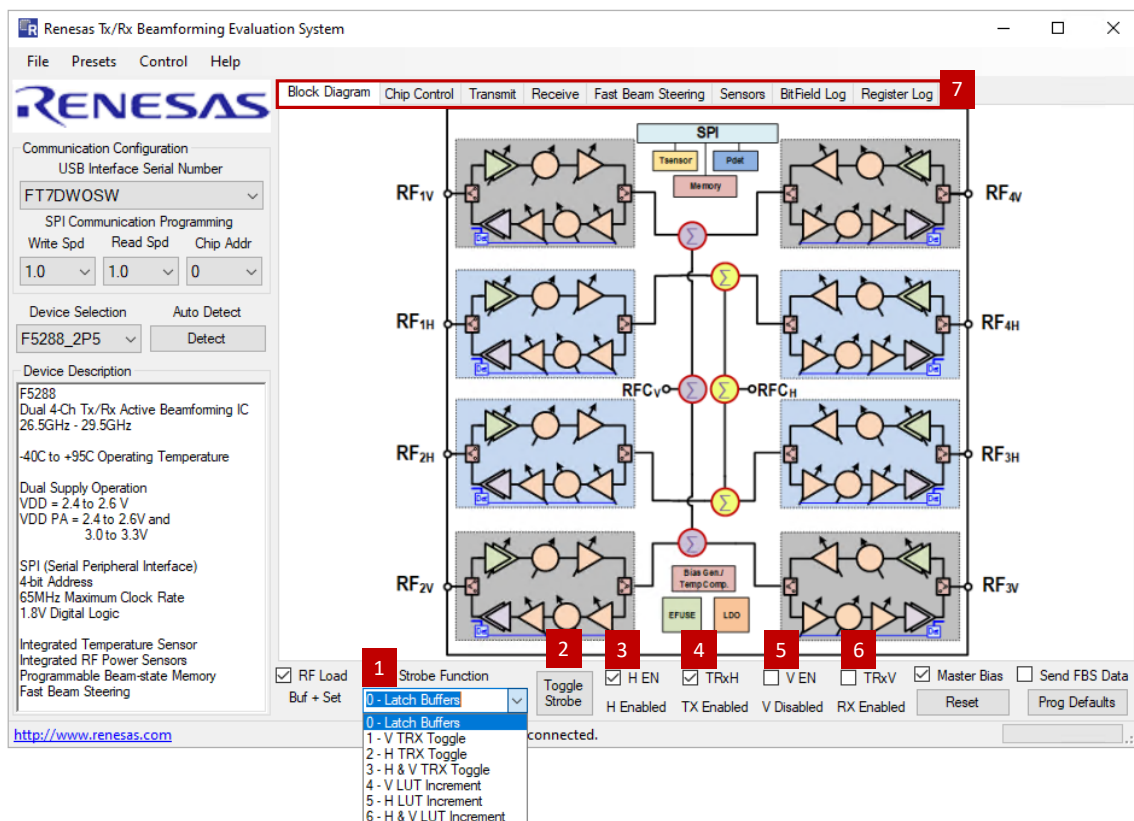


Figure 8. Main Control Buttons

Block Diagram Chip Control Transmit Receive Fast Beam Steering Sensors BitField Log Register Log		
Bias TRX Enable ADC SA Control SRAM		
Name	Control	Description
Master Bias Enable	☐ Disabled	Power Up all bias blocks of the IC.
Bandgap Select	☐ PTAT	Bandgap Select - PTAT generated or Bias generated
PTAT Adjust	4	Internal reference current +/-30% adjust range
PTAT ² Slope	4	PTAT ² Slope Control
SCTAT Enable	☐ Disabled	Super CTAT Bias Enable
SCTAT Trim	0	Super CTAT Bias Trim
SCTAT Control	8	Super CTAT Bias Control

Figure 9. Chip Control Panel: Bias

3.1 Chip Control

The on-chip master bias generator can be enabled/disabled and customized in the Bias subpanel as shown in Figure 9. The TRX Enable subpanel in Figure 10 allows the user to enable/disable different sub-blocks for both TX and RX channels. The Sub Array and SRAM control features are also available in the corresponding subpanels in Figure 11 and Figure 12.

Name	Vertical	Horizontal	Description
RX VGA Enable	☒ Enabled	☒ Enabled	Receiver VGA Enable
RX PS Enable	☒ Enabled	☒ Enabled	Receive Phase Shifter Enable
RX LNA2 Enable	☒ Enabled	☒ Enabled	Receive LNA 2 Enable
RX LNA1 Enable	☒ Enabled	☒ Enabled	Receive LNA 1 Enable
TX VGA1 Enable	☒ Enabled	☒ Enabled	Transmit VGA 1 Enable
TX VGA2 Enable	☒ Enabled	☒ Enabled	Transmit VGA 2 Enable
TX PS Enable	☒ Enabled	☒ Enabled	Transmit Phase Shifter Enable
TX Driver Enable	☒ Enabled	☒ Enabled	Transmit Driver Amplifier Enable
Tx PA Enable	☒ Enabled	☒ Enabled	Transmit Power Amplifier Enable

Figure 10. Chip Control Panel: TRX Enable

Name	Control	Description
SA_Index	0	Sub Array Index

Figure 11. Chip Control Panel: Sub Array Control

Block Diagram			Chip Control			Transmit			Receive			Fast Beam Steering			Sensors			BitField Log			Register Log		
Bias			TRX Enable			ADC			SA Control			SRAM											
Name	Control	Description																					
OSC EN	☐ Disabled	Oscillator Enable																					
SRAM INIT	☐ Idle	Initialize SRAM to Zeros																					
SRAM BIST	☐ Idle	Request SRAM Built In Self Test (BIST)																					
SRAM CRC	☐ Idle	Request SRAM CRC Check Request																					
SRAM SEL	☐ Vertical	Select SRAM Bank for operations 0 = VERTICAL 1 = HORIZONTAL																					
SRAM ERR	Read 0	Number of SRAM BIST Errors (Max 7 reported)																					
SRAM DONE	Read 0	SRAM Access Status (INIT, BIST, or CRC) 0 = REQUESTED 1 = DONE																					
SRAM CRC RESULT	Read 0	SRAM CRC Result																					

Figure 12. Chip Control Panel: SRAM

3.2 Transmit

In the transmit mode, gain and phase settings for each enabled channel can be set in the TX Operation subpanel shown in Figure 13 by using the sliders or directly entering appropriate values. The **LUT En** checkbox (see item 1 in Figure 13) is checked by default to provide 63 steps of gain control for optimal RMS gain error using recommended VGA LUTs. The Gain Mode checkboxes (see item 2 in Figure 13) can be selected for each channel to toggle between 0.25dB and 0.5dB gain step modes. If the **LUT En** checkbox is unchecked, as shown in Figure 14, the gain setting sliders can be adjusted from 0 to 252 (increments of 4, representing the 6 MSBs of gain setting words). The 2 LSBs of gain and phase setting words can be set using items 3 and 4 in Figure 13.

Block Diagram			Chip Control			Transmit			Receive			Fast Beam Steering			Sensors			BitField Log			Register Log		
TX Operation			TX Bias			TX PA			TX DRV			TX PS/VGA											
LUT Mode	Gain Mode	Gain						Phase Shift															
1 ☒ LUT En	☐ Sync	☐ Sync Gain Horizontal Channels						☐ Sync Phase Horizontal Channels															
H1	☒ 0.50dB LSB	< [Slider] > 63						< [Slider] > 0															
H2	☒ 0.50dB LSB	< [Slider] > 63						< [Slider] > 0															
H3	☒ 0.50dB LSB	< [Slider] > 63						< [Slider] > 0															
H4	☒ 0.50dB LSB	< [Slider] > 63						< [Slider] > 0															
	☐ Sync	☐ Sync Gain Vertical Channels						☐ Sync Phase Vertical Channels															
V1	☒ 0.50dB LSB	< [Slider] > 63						< [Slider] > 0															
V2	☒ 0.50dB LSB	< [Slider] > 63						< [Slider] > 0															
V3	☒ 0.50dB LSB	< [Slider] > 63						< [Slider] > 0															
V4	☒ 0.50dB LSB	< [Slider] > 63						< [Slider] > 0															
		Gain Process Correction						Ph Proc Corr		Ph VGA Corr		4											
H	2	3						0		0													
V		3						0		0													

Figure 13. Transmit Panel: TX Operation with VGA LUT Enabled

Block Diagram		Chip Control		Transmit		Receive		Fast Beam Steering		Sensors		BitField Log		Register Log	
TX Operation		TX Bias		TX PA		TX DRV		TX PS/VGA							
LUT Mode	☐ LUT En	Gain Mode	☐ Sync	Gain				Phase Shift							
				☐ Sync Gain Horizontal Channels				☐ Sync Phase Horizontal Channels							
H1	☒ 0.50dB LSB			< [Slider] > 252				< [Slider] > 0							
H2	☒ 0.50dB LSB			< [Slider] > 252				< [Slider] > 0							
H3	☒ 0.50dB LSB			< [Slider] > 252				< [Slider] > 0							
H4	☒ 0.50dB LSB			< [Slider] > 252				< [Slider] > 0							
		☐ Sync		☐ Sync Gain Vertical Channels				☐ Sync Phase Vertical Channels							
V1	☒ 0.50dB LSB			< [Slider] > 252				< [Slider] > 0							
V2	☒ 0.50dB LSB			< [Slider] > 252				< [Slider] > 0							
V3	☒ 0.50dB LSB			< [Slider] > 252				< [Slider] > 0							
V4	☒ 0.50dB LSB			< [Slider] > 252				< [Slider] > 0							
				Gain Process Correction				Ph Proc Corr				Ph VGA Corr			
H				3				0				0			
V				3				0				0			

Figure 14. Transmit Panel: TX Operation with VGA LUT Disabled

The TX channel bias, PA, driver amplifier, phase shifter, and VGA controls for both V and H channels are accessible in corresponding subpanels as shown in Figure 15 to Figure 18, respectively. Recommended settings for specific products are provided for optimal performance.

Block Diagram		Chip Control		Transmit		Receive		Fast Beam Steering		Sensors		BitField Log		Register Log	
TX Operation		TX Bias		TX PA		TX DRV		TX PS/VGA							
Channel	Vertical	☐ Sync Ch Bias Vertical		Horizontal		☐ Sync Ch Bias Horizontal		Description							
Channel Bias CH1	4			4			Ch 1 TX Channel Bias								
Channel Bias CH2	4			4			Ch 2 TX Channel Bias								
Channel Bias CH3	4			4			Ch 3 TX Channel Bias								
Channel Bias CH4	4			4			Ch 4 TX Channel Bias								
SW_BIAS	2			2			Antenna Switch Bias								

Figure 15. Transmit Panel: TX Bias

Block Diagram Chip Control Transmit Receive Fast Beam Steering Sensors BitField Log Register Log			
TX Operation TX Bias TX PA TX DRV TX PS/VGA			
Name	Vertical	Horizontal	Description
TX PA Bias	7	7	Transmit PA core bias
TX PA Cascade Bias	3	3	Transmit PA cascade bias
TX PA Bandgap	☒ Bandgap	☒ Bandgap	Transmit PA bandgap select
TX PA Cascade Cap	0	0	Transmit PA cascade capacitor tuning
TX PA Bias Res	3	3	Transmit PA bias resistor tuning
TX PA RC Feedback	☒ Enabled	☒ Enabled	Transmit PA RC feedback control

Figure 16. Transmit Panel: TX PA

Block Diagram Chip Control Transmit Receive Fast Beam Steering Sensors BitField Log Register Log			
TX Operation TX Bias TX PA TX DRV TX PS/VGA			
Name	Vertical	Horizontal	Description
TX DA Bias	9	9	Transmit DA core bias
TX DA Cascade Bias	6	6	Transmit DA cascade bias
TX DA Bandgap	☒ PTAT ²	☒ PTAT ²	Transmit DA bandgap select
TX DA Input C Tune	0	0	Transmit DA input capacitor tuning
TX PA Inter C Tune	0	0	Transmit DA inter-stage capacitor tuning
TX DA Input R Tune	☐ Disabled	☐ Disabled	Transmit DA input resistor tuning

Figure 17. Transmit Panel: TX DRV

Block Diagram Chip Control Transmit Receive Fast Beam Steering Sensors BitField Log Register Log			
TX Operation TX Bias TX PA TX DRV TX PS/VGA			
Name	Vertical	Horizontal	Description
TX VGA1 Bias	4	4	Transmit VGA1 bias
TX VGA1 PTAT	☒ PTAT ²	☒ PTAT ²	Transmit VGA1 PTAT / PTAT ² select
TX VGA2 Bias	5	5	Transmit VGA2 bias
TX VGA2 PTAT	☐ PTAT	☐ PTAT	Transmit VGA2 PTAT / PTAT ² select
TX PS Bias	4	4	Transmit PS bias
TX PS PTAT	☒ PTAT ²	☒ PTAT ²	Transmit PS PTAT / PTAT ² select

Figure 18. Transmit Panel: TX PS/VGA

3.3 Receive

In the receive mode, gain and phase settings for each enabled channel can be set in the RX Operation subpanel shown in Figure 19 by using the sliders or directly entering appropriate values. Similar to the transmit mode, the **LUT En** checkbox (see item 1 in Figure 19) is checked by default to provide 30 steps of gain control for optimal RMS gain error using recommended VGA LUTs. The Gain Mode checkboxes (see item 2 in Figure 19) can be selected for each channel to toggle between high gain and low gain modes. If the **LUT En** checkbox is unchecked, as shown in Figure 20, the gain setting sliders can be adjusted from 0 to 252 (increments of 4, representing the 6 MSBs of gain setting words). The 2 LSBs of gain and phase setting words can be set using items 3 and 4 in Figure 19.

Block Diagram Chip Control Transmit Receive Fast Beam Steering Sensors BitField Log Register Log			
RX Operation RX Bias RX LNA RX PS/VGA			
LUT Mode	Gain Mode	Gain	Phase Shift
☒ LUT En	☐ Sync	☐ Sync Gain Horizontal Channels	☐ Sync Phase Horizontal Channels
H1	☐ Max Gain	< [Slider] > 30	< [Slider] > 0
H2	☐ Max Gain	< [Slider] > 30	< [Slider] > 0
H3	☐ Max Gain	< [Slider] > 30	< [Slider] > 0
H4	☐ Max Gain	< [Slider] > 30	< [Slider] > 0
V1	☐ Sync	☐ Sync Gain Vertical Channels	☐ Sync Phase Vertical Channels
V2	☐ Max Gain	< [Slider] > 30	< [Slider] > 0
V3	☐ Max Gain	< [Slider] > 30	< [Slider] > 0
V4	☐ Max Gain	< [Slider] > 30	< [Slider] > 0
		Gain Process Correction	Ph Proc Corr Ph VGA Corr
H		3	0 0
V		3	0 0

Figure 19. Receive Panel: RX Operation with VGA LUT Enabled

Block Diagram		Chip Control		Transmit		Receive		Fast Beam Steering		Sensors		BitField Log		Register Log	
RX Operation		RX Bias		RX LNA		RX PS/VGA									
LUT Mode ☐ LUT En		Gain Mode ☐ Sync ☐ Max Gain		Gain ☐ Sync Gain Horizontal Channels				Phase Shift ☐ Sync Phase Horizontal Channels							
H1		☐ Max Gain		☐ Sync Gain Horizontal Channels < [Slider] > 252				< [Slider] > 0							
H2		☐ Max Gain		☐ Sync Gain Horizontal Channels < [Slider] > 252				< [Slider] > 0							
H3		☐ Max Gain		☐ Sync Gain Horizontal Channels < [Slider] > 252				< [Slider] > 0							
H4		☐ Max Gain		☐ Sync Gain Horizontal Channels < [Slider] > 252				< [Slider] > 0							
		☐ Sync		☐ Sync Gain Vertical Channels				☐ Sync Phase Vertical Channels							
V1		☐ Max Gain		☐ Sync Gain Vertical Channels < [Slider] > 252				< [Slider] > 0							
V2		☐ Max Gain		☐ Sync Gain Vertical Channels < [Slider] > 252				< [Slider] > 0							
V3		☐ Max Gain		☐ Sync Gain Vertical Channels < [Slider] > 252				< [Slider] > 0							
V4		☐ Max Gain		☐ Sync Gain Vertical Channels < [Slider] > 252				< [Slider] > 0							
				Gain Process Correction				Ph Proc Corr		Ph VGA Corr					
H				3				0		0					
V				3				0		0					

Figure 20. Receive Panel: RX Operation with VGA LUT Disabled

Block Diagram		Chip Control		Transmit		Receive		Fast Beam Steering		Sensors		BitField Log		Register Log	
RX Operation		RX Bias		RX LNA		RX PS/VGA									
Channel	Vertical	Horizontal	Description												
	☐ Sync Ch Bias Vertical	☐ Sync Ch Bias Horizontal													
Channel Bias CH1	4	4	Ch 1 RX Channel Bias												
Channel Bias CH2	4	4	Ch 2 RX Channel Bias												
Channel Bias CH3	4	4	Ch 3 RX Channel Bias												
Channel Bias CH4	4	4	Ch 4 RX Channel Bias												

Figure 21. Receive Panel: RX Bias

The RX channel bias, LNA, and phase shifter/VGA controls for both V and H channels are available in the corresponding subpanels as shown in Figure 21 to Figure 23, respectively. The RX LNA subpanel in Figure 22 allows the user to test the RX linear mode feature, where gain reduction is performed in steps at the input stage of the RX channel to further improve RX channel linearity.

The LNASW pin provides fast switching of the RX input-stage step attenuator. To enable fast linearity switching through the LNASW pin, select the **Lin Ext Pin Enable** checkbox (in Figure 22).

Block Diagram	Chip Control	Transmit	Receive	Fast Beam Steering	Sensors	BitField Log	Register Log
RX Operation	RX Bias	RX LNA	RX PS/VGA				

Name	Control		Description
LNASW PIN (GPIO)	☐ Linearity Mode (0)		LNASW GPIO Hardware Linearity Control Pin Enabled/Disabled
Name	Vertical	Horizontal	Description
Lin Ext Pin Enable	☐ Ext Pin Disabled	☐ Ext Pin Disabled	External Linearity Pin Enable
Linearity Mode Sel	0: Max Gain ▾	0: Max Gain ▾	LNA Linearity Control
LNA 1 Bias	5 ▾	5 ▾	LNA 1 Bias Current
LNA 1 PTAT Select	☒ PTAT ²	☒ PTAT ²	LNA 1 PTAT Select 0 = PTAT 1 = PTAT ²
LNA 2 Bias	3 ▾	3 ▾	LNA 2 Bias Current Setting
LNA 2 PTAT Select	☒ PTAT ²	☒ PTAT ²	LNA 2 PTAT Select 0 = PTAT 1 = PTAT ²

Figure 22. Receive Panel: RX LNA

Block Diagram	Chip Control	Transmit	Receive	Fast Beam Steering	Sensors	BitField Log	Register Log
RX Operation	RX Bias	RX LNA	RX PS/VGA				

Name	Vertical	Horizontal	Description
RX PS BIAS	4 ▾	4 ▾	RX Phase Shifter Bias Current
RX PS PTAT	☒ PTAT ²	☒ PTAT ²	RX Phase Shifter PTAT Select 0 = PTAT 1 = PTAT ²
RX VGA BIAS	4 ▾	4 ▾	RX VGA Bias Current Setting
RX VGA PTAT	☐ PTAT	☐ PTAT	RX VGA PTAT Select 0 = PTAT 1 = PTAT ²

Figure 23. Receive Panel: RX PS/VGA

3.4 Fast Beam Steering

FBS allows fast programming to a specific beam state. The device has two dedicated LUTs (VLUT and HLUT), for vertical and horizontal polarization respectively, with 1024 beam states each. A single LUT address points to four 16-bit register locations (equivalent to four channels) that contain programmable phase and gain settings. The phase and gain settings for 1 LUT entry constitute a beam state. Each beam state can be either TX or RX, and once selected, LUT data will be loaded simultaneously to all four channels.

Name	Vertical	Horizontal	Description
Ch 1 Enable	☒ Enabled	☒ Enabled	Channel 1 Enable when CONTROL V_EN or H_EN is TRUE
Ch 2 Enable	☒ Enabled	☒ Enabled	Channel 2 Enable when CONTROL V_EN or H_EN is TRUE
Ch 3 Enable	☒ Enabled	☒ Enabled	Channel 3 Enable when CONTROL V_EN or H_EN is TRUE
Ch 4 Enable	☒ Enabled	☒ Enabled	Channel 4 Enable when CONTROL V_EN or H_EN is TRUE
LUT Pointer	1023	1023	Updates GAIN/PHASE registers with LUT Table Data
TRx	☐ RXV Enabled	☐ RXH Enabled	Polarization Enable
GUI LUT Pointer Update	☒ Automatic LUT Pointer Update		GUI Control of LUT Pointer. Gain and phase values stored in LUT indexes 0x3FE-0x3FF. Update LUT Pointer with TRx_V and TRx_H

Figure 24. Fast Beam Steering Panel: LUT Configuration

The LUT Configuration subpanel in Figure 24 allows users to quickly enable/disable specific channels for both horizontal and vertical polarizations. The **Automatic LUT Pointer Update** checkbox should always be selected so that the GUI will control and automatically update the LUT pointer. In manual operations, the GUI will store gain and phase values in the LUT indexes 1022 (for TX) and 1023 (for RX), which will be automatically updated with TRxV and TRxH settings.

If the FBS LUT data is programmed to the SRAM, fast beam steering can be performed using the **LUT Index Selection** slider or by directly entering the index number (0 to 1023) in the entry box (see item 5 in Figure 25) in the LUT Entry Select subpanel. The FBS LUT data on SRAM can also be edited on the SRAM Editor subpanel shown in Figure 26. Select the **Enable Edit** checkbox (see item 1 in Figure 26), polarization (see item 2 in Figure 26), and LUT Index to be edited (see item 3 in Figure 26). Then click the **Program Index to Device** button to write the gain and phase settings (see item 4 in Figure 26) to SRAM at the specified LUT index. As an example, the LUT Entry Select subpanel in Figure 26 displays the values programmed to the SRAM after the update.

TRX Sel	HV Sel	Prog Mode	FBS Programming	FBS Buffer	Toggle Enable	SA Enable
☒ Transmit (1)	☒ Horizontal (2)	☒ Local (3)	☒ Auto Send (4)	☒ FBS Immediate	☐ Toggle Disabled	☐ Global
☐ Receive	☐ Vertical	☐ Global	Update Now	Toggle Now	End Toggle	0

LUT Index Selection (5): 0

Field	Chan 1	Chan 2	Chan 3	Chan 4
PS_SET				
VGA_SET				

Figure 25. Fast Beam Steering Panel: LUT Entry Select

Index	Field	Chan 1	Chan 2	Chan 3	Chan 4
PS_SET		0	0	0	0
VGA_SET		255	255	255	255

Values Read Back From SRAM After Activation (6):

Field	Chan 1	Chan 2	Chan 3	Chan 4
PS_SET	0	0	0	0
VGA_SET	255	255	255	255

Figure 26. Fast Beam Steering Panel: SRAM Editor

3.5 Sensors

The F5268/F5288 has integrated temperature sensors and power detectors for each TX channel. For temperature sensors, calibration must be performed at one known temperature only to find the value of *Offset* for every chip based on the following equation.

$$T_{Sens} = 0.7715 \times Sensor + Offset$$

For example, with the chip in standby mode where the master bias is enabled but all RF channels are OFF, at a known ambient temperature (T_{Amb}), T_{Sens} should be approximately T_{Amb} . By clicking the **Measure** buttons and reading the *Sensor* value (**ADC Output**) in the Temperature subpanel shown in Figure 27, users can calculate the value of *Offset* (**b** in Figure 27) such that T_{Sens} (**f(x)** in Figure 27) is approximately T_{Amb} .

A typical value for *Offset* is -263. A lower estimation accuracy of $\pm 25^{\circ}\text{C}$ is expected if this value is used for all chips without any calibration.

Block Diagram

Chip Control

Transmit

Receive

Fast Beam Steering

Sensors

BitField Log

Register Log

Sensor Macros

PDET Configuration

Enable

Bias

PCM

Temperature

Power Detector

Channel	Individual Measurement	ADC Output (x)	m	b	f(x)	Unit
CORE	Measure	0	0.7715	-300.0	0.0	°C
	Measure H					
TxH1	Measure	0	0.7715	-300.0	0.0	°C
TxH2	Measure	0	0.7715	-300.0	0.0	°C
TxH3	Measure	0	0.7715	-300.0	0.0	°C
TxH4	Measure	0	0.7715	-300.0	0.0	°C
	Measure V					
TxV1	Measure	0	0.7715	-300.0	0.0	°C
TxV2	Measure	0	0.7715	-300.0	0.0	°C
TxV3	Measure	0	0.7715	-300.0	0.0	°C
TxV4	Measure	0	0.7715	-300.0	0.0	°C

Figure 27. Sensors: Temperature

The Power Detector subpanel shown in Figure 28 allows users to quickly evaluate the on-chip TX power detectors, measuring the TX output power of each channel. The power detector operates over a wide power range and with continuous-wave or modulated signals. The following formula is used to estimate the average RF output power in dBm. For recommended values of **Constant** and **Coefficient**, please see the latest F5268 and F5288 datasheets.

$$P_{TX} = \text{Constant} + \text{Coefficient} \times 10\text{Log}_{10}\left(\frac{\text{Sensor}}{1023}\right)$$

Block Diagram

Chip Control

Transmit

Receive

Fast Beam Steering

Sensors

BitField Log

Register Log

Sensor Macros

PDET Configuration

Enable

Bias

PCM

Temperature

Power Detector

Channel	Individual Measurement	ADC Output	Constant	Coefficient	Log Result	Unit
	Measure H					
TxH1	Measure H1	0	20.12	1.005	-inf	dBm
TxH2	Measure H2	0	20.12	1.005	-inf	dBm
TxH3	Measure H3	0	20.12	1.005	-inf	dBm
TxH4	Measure H4	0	20.12	1.005	-inf	dBm
	Measure V					
TxV1	Measure V1	0	20.12	1.005	-inf	dBm
TxV2	Measure V2	0	20.12	1.005	-inf	dBm
TxV3	Measure V3	0	20.12	1.005	-inf	dBm
TxV4	Measure V4	0	20.12	1.005	-inf	dBm

Figure 28. Sensors: Power Detector

3.6 Bit Field Log and Register Log

To use the Bit Field Log and Register Log features, select the **Enable Bit Field Log** and **Enable Register Log** checkboxes in Figure 29 and Figure 30.

Block Diagram					
Chip Control					
Transmit					
Receive					
Fast Beam Steering					
Sensors					
BitField Log					
Register Log					
Time Stamp	RD/WR	SPI Addr	Device Field Name	Value	
031323 14:37:22:09	WRITE	0x00	RXH_GAIN_MODE_2	0x0000	
031323 14:37:22:09	WRITE	0x00	TXH_CH_BIAS_2	0x0004	
031323 14:37:22:09	WRITE	0x00	TXH_GAIN_MODE_2	0x0001	
031323 14:37:22:09	WRITE	0x00	RXH_PHASE_CTRL_3	0x0000	
031323 14:37:22:09	WRITE	0x00	TXH_PHASE_CTRL_3	0x0000	
031323 14:37:22:09	WRITE	0x00	RXH_CH_BIAS_3	0x0004	
031323 14:37:22:09	WRITE	0x00	RXH_GAIN_MODE_3	0x0000	
031323 14:37:22:09	WRITE	0x00	TXH_CH_BIAS_3	0x0004	
031323 14:37:22:09	WRITE	0x00	TXH_GAIN_MODE_3	0x0001	
031323 14:37:22:09	WRITE	0x00	RXH_PHASE_CTRL_4	0x0000	
031323 14:37:22:09	WRITE	0x00	TXH_PHASE_CTRL_4	0x0000	
031323 14:37:22:09	WRITE	0x00	RXH_CH_BIAS_4	0x0004	
031323 14:37:22:09	WRITE	0x00	RXH_GAIN_MODE_4	0x0000	
031323 14:37:22:10	WRITE	0x00	TXH_CH_BIAS_4	0x0004	
031323 14:37:22:10	WRITE	0x00	TXH_GAIN_MODE_4	0x0001	
031323 14:37:22:10	WRITE	0x00	V1_EN	0x0001	
031323 14:37:22:10	WRITE	0x00	V2_EN	0x0001	
031323 14:37:22:10	WRITE	0x00	V3_EN	0x0001	
031323 14:37:22:10	WRITE	0x00	V4_EN	0x0001	
031323 14:37:22:10	WRITE	0x00	VLUT_PTR	0x03FF	
031323 14:37:22:10	WRITE	0x00	VLUT_TRN	0x0000	
031323 14:37:22:10	WRITE	0x00	H1_EN	0x0001	
031323 14:37:22:10	WRITE	0x00	H2_EN	0x0001	
031323 14:37:22:10	WRITE	0x00	H3_EN	0x0001	
031323 14:37:22:10	WRITE	0x00	H4_EN	0x0001	
031323 14:37:22:10	WRITE	0x00	HLUT_PTR	0x03FF	
031323 14:37:22:10	WRITE	0x00	HLUT_TRN	0x0000	

Write All To Device Read All From Device ☒ Enable BitField Log Clear Log Save Log

Figure 29. Bit Field Log

Block Diagram					
Chip Control					
Transmit					
Receive					
Fast Beam Steering					
Sensors					
BitField Log					
Register Log					
Time Stamp	RD/WR	SPI Addr	Register Address	Value	
031323 14:38:24:08	WRITE	0x00	0x47	0x000C	
031323 14:38:24:10	WRITE	0x00	0x48	0x00FF	
031323 14:38:24:13	WRITE	0x00	0x49	0x00FF	
031323 14:38:24:16	WRITE	0x00	0x4A	0x0004	
031323 14:38:24:17	WRITE	0x00	0x4B	0x000C	
031323 14:38:24:19	WRITE	0x00	0x4C	0x00FF	
031323 14:38:24:22	WRITE	0x00	0x4D	0x00FF	
031323 14:38:24:25	WRITE	0x00	0x4E	0x0004	
031323 14:38:24:27	WRITE	0x00	0x4F	0x000C	
031323 14:38:24:28	WRITE	0x00	0x50	0x00FF	
031323 14:38:24:32	WRITE	0x00	0x51	0x00FF	
031323 14:38:24:35	WRITE	0x00	0x52	0x0004	
031323 14:38:24:36	WRITE	0x00	0x53	0x000C	
031323 14:38:24:38	WRITE	0x00	0x54	0x00FF	
031323 14:38:24:41	WRITE	0x00	0x55	0x00FF	
031323 14:38:24:44	WRITE	0x00	0x56	0x0004	
031323 14:38:24:46	WRITE	0x00	0x57	0x000C	
031323 14:38:24:47	WRITE	0x00	0x58	0x00FF	
031323 14:38:24:50	WRITE	0x00	0x59	0x00FF	
031323 14:38:24:53	WRITE	0x00	0x5A	0x0004	
031323 14:38:24:55	WRITE	0x00	0x5B	0x000C	
031323 14:38:24:56	WRITE	0x00	0x5C	0x00FF	
031323 14:38:24:59	WRITE	0x00	0x5D	0x00FF	
031323 14:38:24:63	WRITE	0x00	0x5E	0x0004	
031323 14:38:24:64	WRITE	0x00	0x5F	0x000C	
031323 14:38:24:66	WRITE	0x00	0x01	0x3FFF	
031323 14:38:24:67	WRITE	0x00	0x02	0x3FFF	

Write All To Device Read All From Device ☒ Enable Register Log Clear Log Save Log

Figure 30. Register Log

4. Example Procedures

The following examples provide guidelines on how to use the software GUI to control channel operations.

4.1 Enable All Vertical TX Channels and Disable All Horizontal Channels

1. Reset to program defaults using the **Toggle Reset** button (item 5 in Figure 5) as explained in Section 2.4.
2. Chip Control Tab -> Bias Tab -> Master Bias Enable = Enabled (checked, Figure 9).
3. H EN (bottom of the main GUI panel) = H Disabled (unchecked, item 3 in Figure 8).
4. V EN (bottom of the main GUI panel) = V Enabled (checked, item 5 in Figure 8).
5. TRxV (bottom of the main GUI panel) = TX Enabled (checked, item 6 in Figure 8).
6. Fast Beam Steering Tab -> LUT Config Tab -> Vertical Ch 1 Enable = Enabled (checked, Figure 24).
7. Fast Beam Steering Tab -> LUT Config Tab -> Vertical Ch 2 Enable = Enabled (checked, Figure 24).
8. Fast Beam Steering Tab -> LUT Config Tab -> Vertical Ch 3 Enable = Enabled (checked, Figure 24).
9. Fast Beam Steering Tab -> LUT Config Tab -> Vertical Ch 4 Enable = Enabled (checked, Figure 24).
10. Transmit Tab -> TX Operation Tab -> V1 Gain = 63 or any desired value (Figure 13).
11. Transmit Tab -> TX Operation Tab -> V2 Gain = 63 or any desired value (Figure 13).
12. Transmit Tab -> TX Operation Tab -> V3 Gain = 63 or any desired value (Figure 13).
13. Transmit Tab -> TX Operation Tab -> V4 Gain = 63 or any desired value (Figure 13).
14. Transmit Tab -> TX Operation Tab -> V1 Phase Shift = 0 or any desired value (Figure 13).
15. Transmit Tab -> TX Operation Tab -> V2 Phase Shift = 0 or any desired value (Figure 13).
16. Transmit Tab -> TX Operation Tab -> V3 Phase Shift = 0 or any desired value (Figure 13).
17. Transmit Tab -> TX Operation Tab -> V4 Phase Shift = 0 or any desired value (Figure 13).
18. Note changes in current and RF gain.

4.2 Enable a Single Horizontal TX Channel (Channel 1) and Disable All Vertical Channels

1. Reset to program defaults using the **Toggle Reset** button (item 5 in Figure 5) as explained in Section 2.4.
2. Chip Control Tab -> Bias Tab -> Master Bias Enable = Enabled (checked, Figure 9).
3. V EN (bottom of the main GUI panel) = V Disabled (unchecked, item 5 in Figure 8).
4. H EN (bottom of the main GUI panel) = H Enabled (checked, item 3 in Figure 8).
5. TRxH (bottom of the main GUI panel) = TX Enabled (checked, item 4 in Figure 8).
6. Fast Beam Steering Tab -> LUT Config Tab -> Horizontal Ch 1 Enable = Enabled (checked, Figure 24).
7. Fast Beam Steering Tab -> LUT Config Tab -> Horizontal Ch 2 Enable = Disabled (unchecked, Figure 24).
8. Fast Beam Steering Tab -> LUT Config Tab -> Horizontal Ch 3 Enable = Disabled (unchecked, Figure 24).
9. Fast Beam Steering Tab -> LUT Config Tab -> Horizontal Ch 4 Enable = Disabled (unchecked, Figure 24).
10. Transmit Tab -> TX Operation Tab -> H1 Gain = 63 or any desired value (Figure 13).
11. Transmit Tab -> TX Operation Tab -> H1 Phase Shift = 0 or any desired value (Figure 13).
12. Note changes in current and RF gain.

4.3 Enable a Single Vertical RX Channels (Channel 3) and Disable All Horizontal Channels

1. Reset to program defaults using the **Toggle Reset** button (item 5 in Figure 5) as explained in Section 2.4.
2. Chip Control Tab -> Bias Tab -> Master Bias Enable = Enabled (checked, Figure 9).
3. H EN (bottom of the main GUI panel) = H Disabled (unchecked, item 3 in Figure 8).
4. V EN (bottom of the main GUI panel) = V Enabled (checked, item 5 in Figure 8).
5. TRxV (bottom of the main GUI panel) = RX Enabled (unchecked, item 6 in Figure 8).
6. Fast Beam Steering Tab -> LUT Config Tab -> Vertical Ch 1 Enable = Disabled (unchecked, Figure 24).
7. Fast Beam Steering Tab -> LUT Config Tab -> Vertical Ch 2 Enable = Disabled (unchecked, Figure 24).
8. Fast Beam Steering Tab -> LUT Config Tab -> Vertical Ch 3 Enable = Enabled (checked, Figure 24).
9. Fast Beam Steering Tab -> LUT Config Tab -> Vertical Ch 4 Enable = Disabled (unchecked, Figure 24).
10. Receive Tab -> RX Operation Tab -> V3 Gain = 30 or any desired value (Figure 19).
11. Receive Tab -> RX Operation Tab -> V3 Phase Shift = 0 or any desired value (Figure 19).
12. Note changes in current and RF gain.

4.4 Enable All Horizontal RX Channels and Disable All Vertical Channels, then Switch to Enable only Vertical TX Channel 4 and Disable All Horizontal Channels

1. Reset to program defaults using the **Toggle Reset** button (item 5 in Figure 5) as explained in Section 2.4.
2. Chip Control Tab -> Bias Tab -> Master Bias Enable = Enabled (checked, Figure 9).
3. V EN (bottom of the main GUI panel) = V Disabled (unchecked, item 5 in Figure 8).
4. H EN (bottom of the main GUI panel) = H Enabled (checked, item 3 in Figure 8).
5. TRxH (bottom of the main GUI panel) = RX Enabled (unchecked, item 4 in Figure 8).
6. Fast Beam Steering Tab -> LUT Config Tab -> Horizontal Ch 1 Enable = Enabled (checked, Figure 24).
7. Fast Beam Steering Tab -> LUT Config Tab -> Horizontal Ch 2 Enable = Enabled (checked, Figure 24).
8. Fast Beam Steering Tab -> LUT Config Tab -> Horizontal Ch 3 Enable = Enabled (checked, Figure 24).
9. Fast Beam Steering Tab -> LUT Config Tab -> Horizontal Ch 4 Enable = Enabled (checked, Figure 24).
10. Receive Tab -> RX Operation Tab -> H1 Gain = 30 or any desired value (Figure 19).
11. Receive Tab -> RX Operation Tab -> H2 Gain = 30 or any desired value (Figure 19).
12. Receive Tab -> RX Operation Tab -> H3 Gain = 30 or any desired value (Figure 19).
13. Receive Tab -> RX Operation Tab -> H4 Gain = 30 or any desired value (Figure 19).
14. Receive Tab -> RX Operation Tab -> H1 Phase Shift = 0 or any desired value (Figure 19).
15. Receive Tab -> RX Operation Tab -> H2 Phase Shift = 0 or any desired value (Figure 19).
16. Receive Tab -> RX Operation Tab -> H3 Phase Shift = 0 or any desired value (Figure 19).
17. Receive Tab -> RX Operation Tab -> H4 Phase Shift = 0 or any desired value (Figure 19).
18. Note increase in current and RF gain, then switch to enable only vertical TX channel 4 as follows.
19. H EN (bottom of the main GUI panel) = H Disabled (unchecked, item 3 in Figure 8).
20. V EN (bottom of the main GUI panel) = V Enabled (checked, item 5 in Figure 8).
21. TRxV (bottom of the main GUI panel) = TX Enabled (checked, item 6 in Figure 8).
22. Fast Beam Steering Tab -> LUT Config Tab -> Vertical Ch 1 Enable = Disabled (unchecked, Figure 24).

23. Fast Beam Steering Tab -> LUT Config Tab -> Vertical Ch 2 Enable = Disabled (unchecked, Figure 24).
24. Fast Beam Steering Tab -> LUT Config Tab -> Vertical Ch 3 Enable = Disabled (unchecked, Figure 24).
25. Fast Beam Steering Tab -> LUT Config Tab -> Vertical Ch 4 Enable = Enabled (checked, Figure 24).
26. Transmit Tab -> TX Operation Tab -> V4 Gain = 63 or any desired value (Figure 13).
27. Transmit Tab -> TX Operation Tab -> V4 Phase Shift = 0 or any desired value (Figure 13).
28. Note changes in current and RF gain.

4.5 Fast Beam Steering with All Vertical TX Channels Enable in Local Programming Mode

1. Reset to program defaults using the **Toggle Reset** button (item 5 in Figure 5) as explained in Section 2.4.
2. Select the **Send FBS Data** checkbox (item 7 in Figure 5).
3. From the **File** menu, select **Load Fast Beam Steering Lookup Table** (item 3 in Figure 7) and proceed to choose the desired FBS LUT file (.csv).
4. Click the **Program Defaults** button (item 6 in Figure 5).
5. Chip Control Tab -> Bias Tab -> Master Bias Enable = Enabled (checked, Figure 9).
6. H EN (bottom of the main GUI panel) = H Disabled (unchecked, item 3 in Figure 8).
7. V EN (bottom of the main GUI panel) = V Enabled (checked, item 5 in Figure 8).
8. TRxV (bottom of the main GUI panel) = TX Enabled (checked, item 6 in Figure 8).
9. Fast Beam Steering Tab -> LUT Config Tab -> Vertical Ch 1 Enable = Enabled (checked, Figure 24).
10. Fast Beam Steering Tab -> LUT Config Tab -> Vertical Ch 2 Enable = Enabled (checked, Figure 24).
11. Fast Beam Steering Tab -> LUT Config Tab -> Vertical Ch 3 Enable = Enabled (checked, Figure 24).
12. Fast Beam Steering Tab -> LUT Config Tab -> Vertical Ch 4 Enable = Enabled (checked, Figure 24).
13. Fast Beam Steering Tab -> LUT Entry Select Tab -> TRX Sel = Transmit (item 1 in Figure 25).
14. Fast Beam Steering Tab -> LUT Entry Select Tab -> HV Sel = Vertical Polarization (item 2 in Figure 25).
15. Fast Beam Steering Tab -> LUT Entry Select Tab -> Prog Mode = Local (item 3 in Figure 25).
16. Fast Beam Steering Tab -> LUT Entry Select Tab -> SPI Programming = Auto Send (checked, item 4 in Figure 25)
17. Fast Beam Steering Tab -> LUT Entry Select Tab -> LUT Index Selection = any desired LUT index using the slider or the entry box (item 5 in Figure 25).
18. Note changes in the SRAM read-back display (item 6 in Figure 25).
19. Note changes in current and RF gain.

5. PCB Guidelines

5.1 Schematics

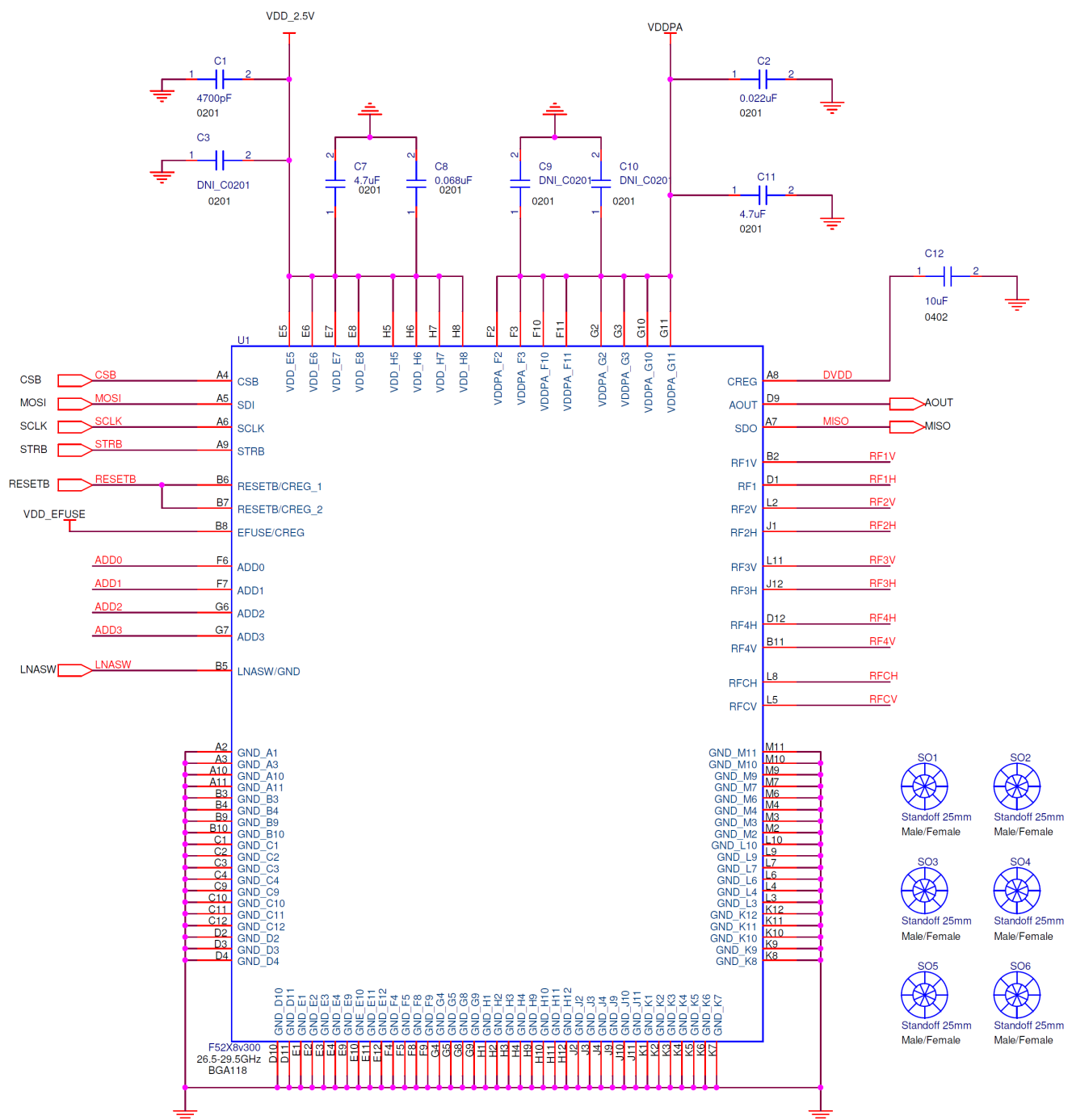
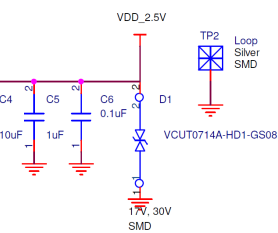
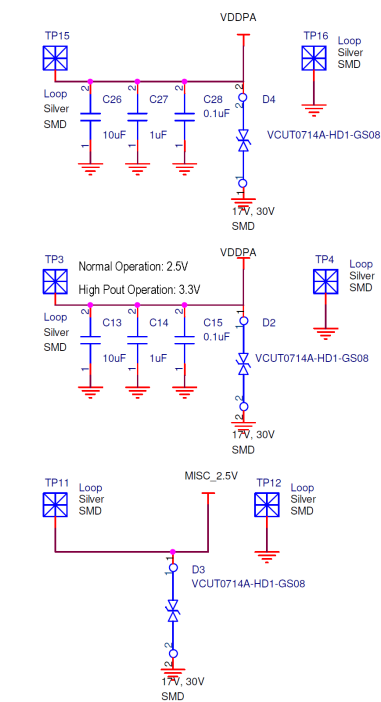


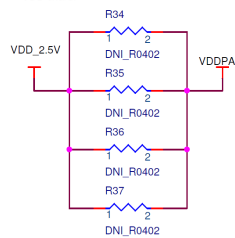
Figure 31. F5268/F5288 Evaluation Board Schematic – Part 1

POWER SUPPLY



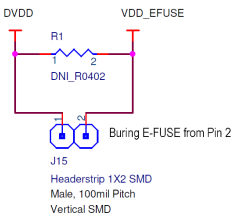
SHARE VDD & VDDPA

If only one power supply is used, please implement below 0-ohm resistors to allow VDD share.

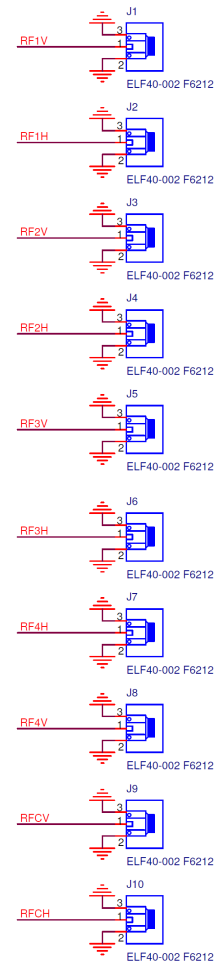


VDD_EFUSE SELECTION

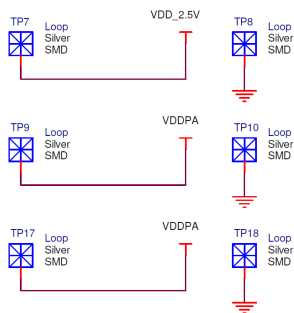
Once the E-Fuse is burnt, please put a jumper in and E-Fuse will connect to DVDD provided by the DUT.



RF Connectors



Voltage Sensing



SELECTION OF ADDRESS PINS

Address pins can be controlled by MCU by place the corresponding resistors and remove the corresponding resistors to ground.

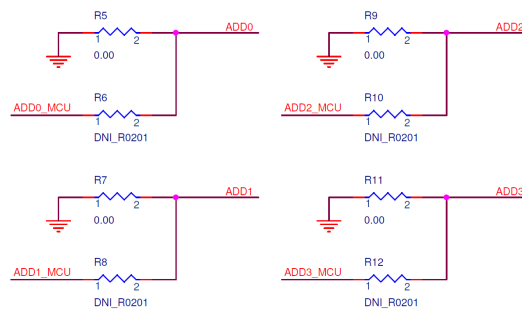


Figure 32. F5268/F5288 Evaluation Board Schematic – Part 2

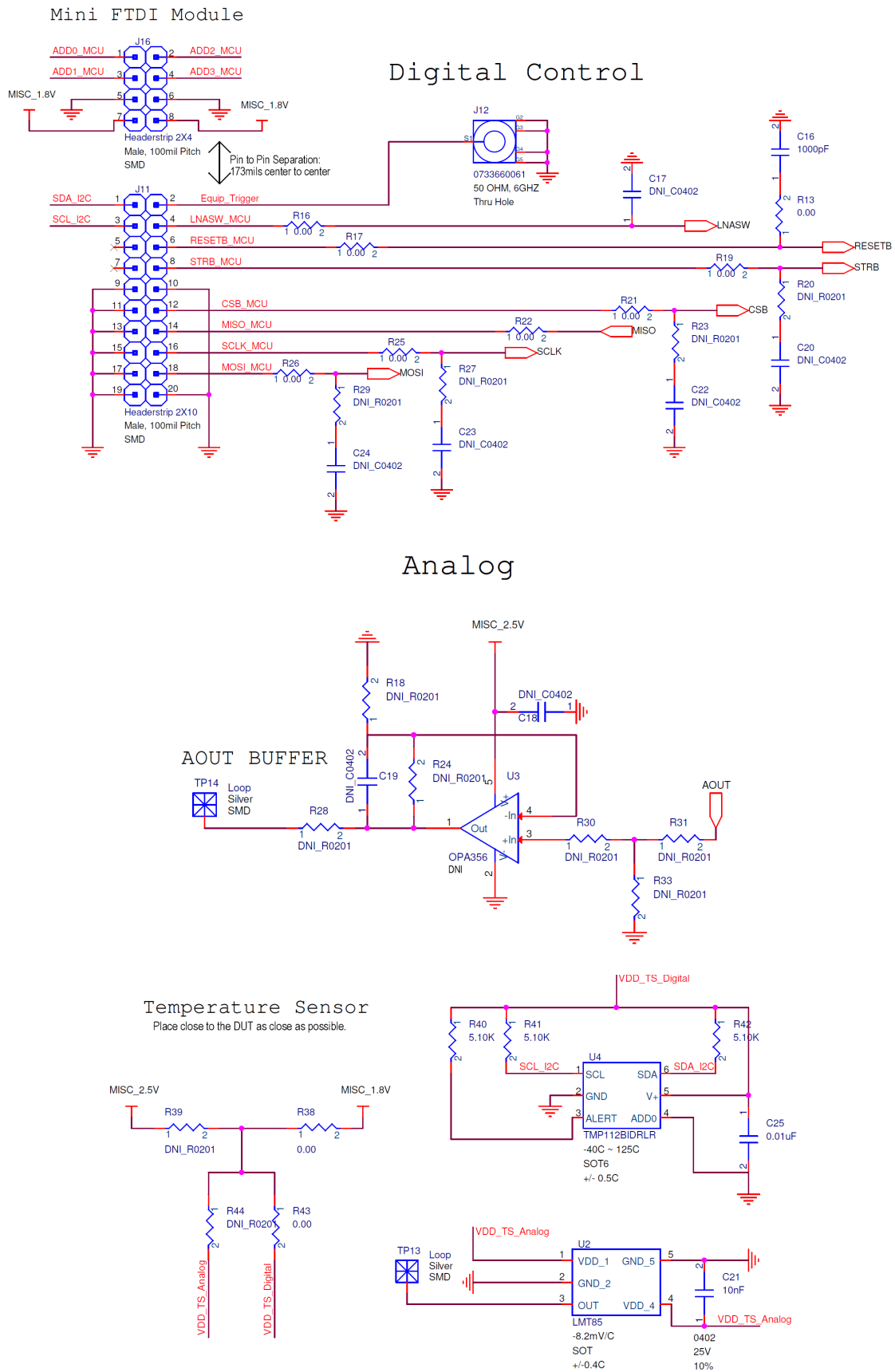


Figure 33. F5268/F5288 Evaluation Board Schematic – Part 3

6. Ordering Information

Part Number	Description
RTKA81F5268ST000RU	F5268 Evaluation System Kit
RTKA81F5288ST000RU	F5288 Evaluation System Kit
F5268/F5288 THRU Board	F5268/F5288 THRU Board. Please contact Renesas sales to purchase the THRU board.

7. Revision History

Revision	Revision Date	Description of Change
1.00	Jun 26, 2023	Updated evaluation system software (R0.1.2.0)
0.04	Nov 23, 2021	- Revised EVS information (Rev. A3) for F5268/F5288 v300 and a new control software - Updated document to the latest template - Completed other minor changes
0.03	Aug 11, 2020	Corrected EVB schematic pin names to be consistent with the datasheet.
0.02	Jul 19, 2020	Revise F5288 EVBs (Rev. B).
0.01	Dec 06, 2019	Initial release.