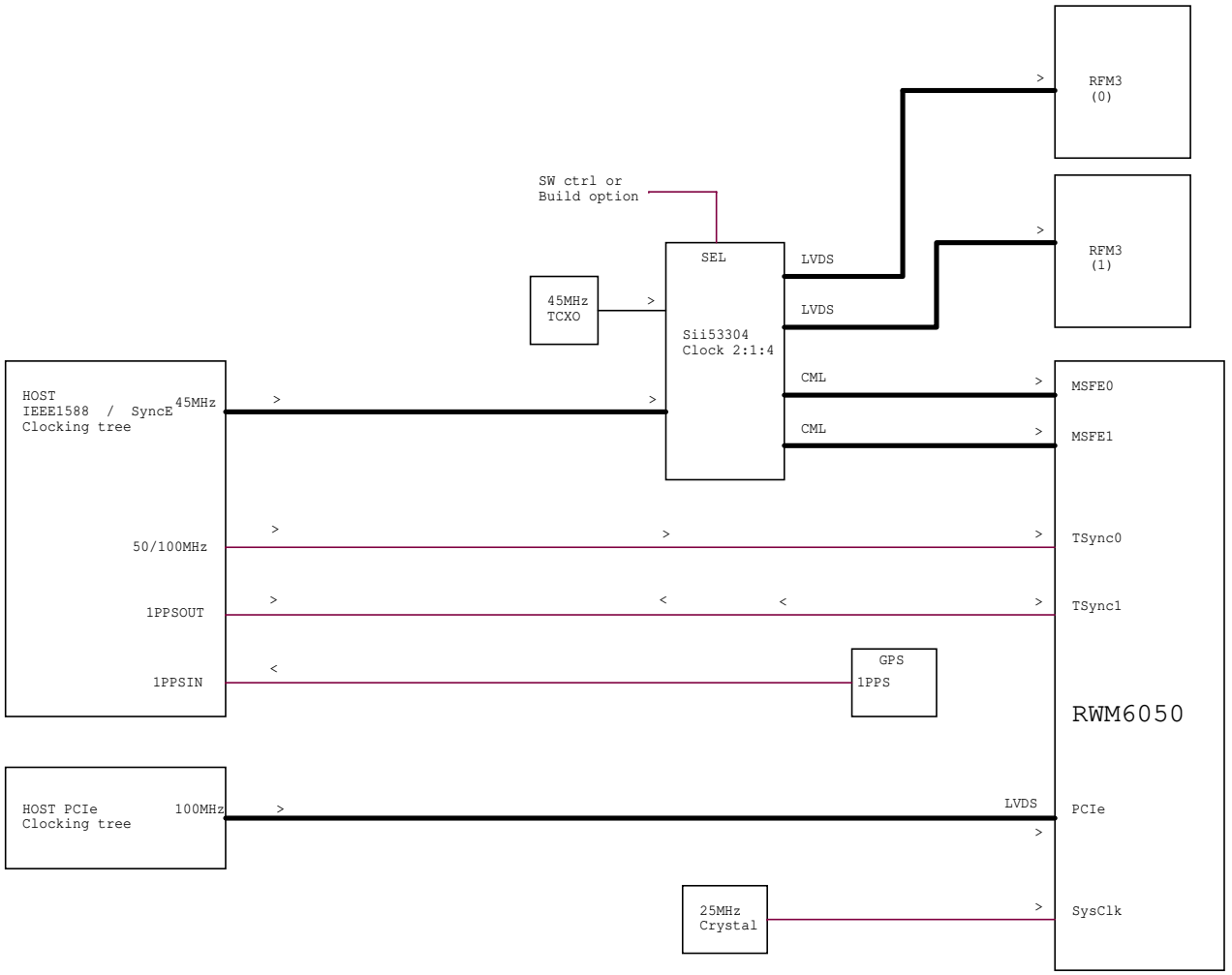

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Board Title	RWM6050 Example Design
Sheet Title	Block diagram - Clocking scheme
Build	Example reference
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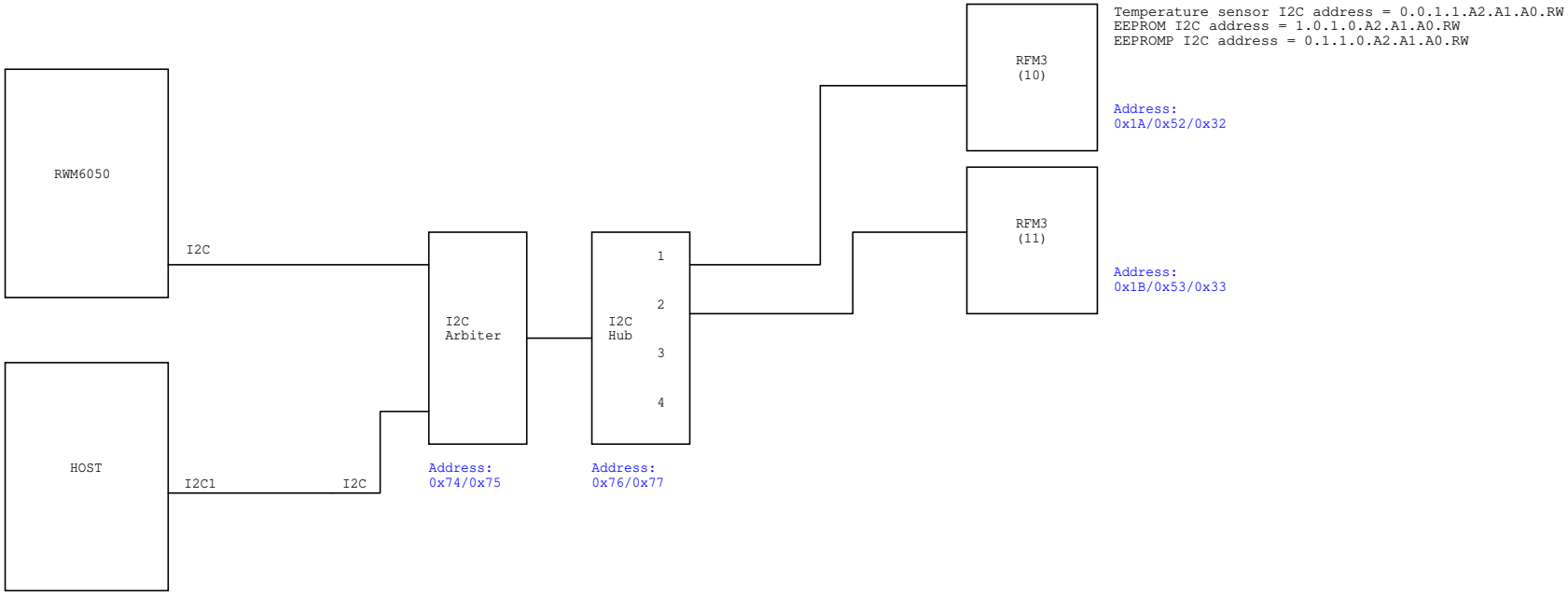

I2C ADDRESSES:

0x19
0x1A RFM3 (10) = SE97B
0x1B RFM3 (11) = SE97B
0x1C
0x1D
0x1E
0x1F
0x2C
0x30
0x31
0x32 RFM3 (10) = SE97B
0x33 RFM3 (11) = SE97B
0x34
0x35
0x36
0x37
0x50
0x51
0x52 RFM3 (10) = SE97B
0x53 RFM3 (11) = SE97B
0x54
0x55
0x56
0x57
0x5F
0x70
0x71
0x72
0x73
0x74 Arbiter (I2CA0=0)
0x75 Arbiter (I2CA0=1)
0x76 Hub (I2CA0=0)
0x77 Hub (I2CA0=1)
0x78 – 0x7B RESERVED

Board Title	RWM6050 Example Design
Sheet Title	Block diagram - I2C connectivity
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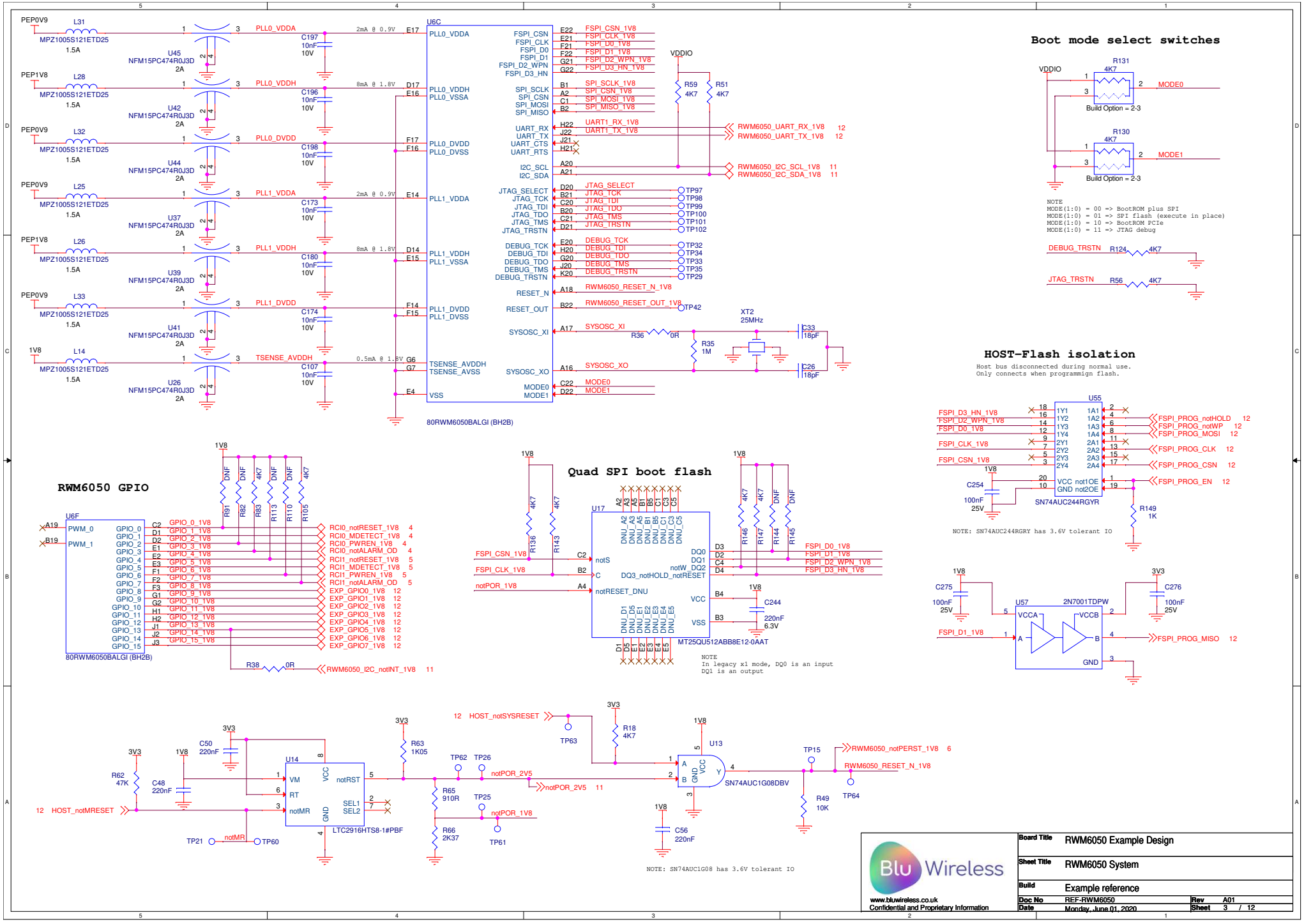
Boot mode select switches
VDDIO
R131
4K7
MODE0
Build Option = 2-3
R130
4K7
MODE1
Build Option = 2-3
NOTE
MODE(1:0) = 00 => BootROM plus SPI
MODE(1:0) = 01 => SPI flash (execute in place)
MODE(1:0) = 10 => BootROM PCIe
MODE(1:0) = 11 => JTAG debug
DEBUG_TRSTN R124 4K7
JTAG_TRSTN R56 4K7
HOST-Flash isolation
Host bus disconnected during normal use.
Only connects when programmign flash.
U55
SN74AUC244RGYR
NOTE: SN74AUC244RGRY has 3.6V tolerant IO
RWM6050 GPIO
U6F
80RWM6050BALGI (BH2B)
Quad SPI boot flash
U17
MT25QU512ABB8E12-0AAT
NOTE
In legacy x1 mode, DQ0 is an input
DQ1 is an output
U57
2N7001TDPW
U6C
80RWM6050BALGI (BH2B)
U14
LTC2916HTS8-1#PBF
U13
SN74AUC1G08DBV
NOTE: SN74AUC1G08 has 3.6V tolerant IO
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Board Title RWM6050 Example Design
Sheet Title RWM6050 System
Build Example reference
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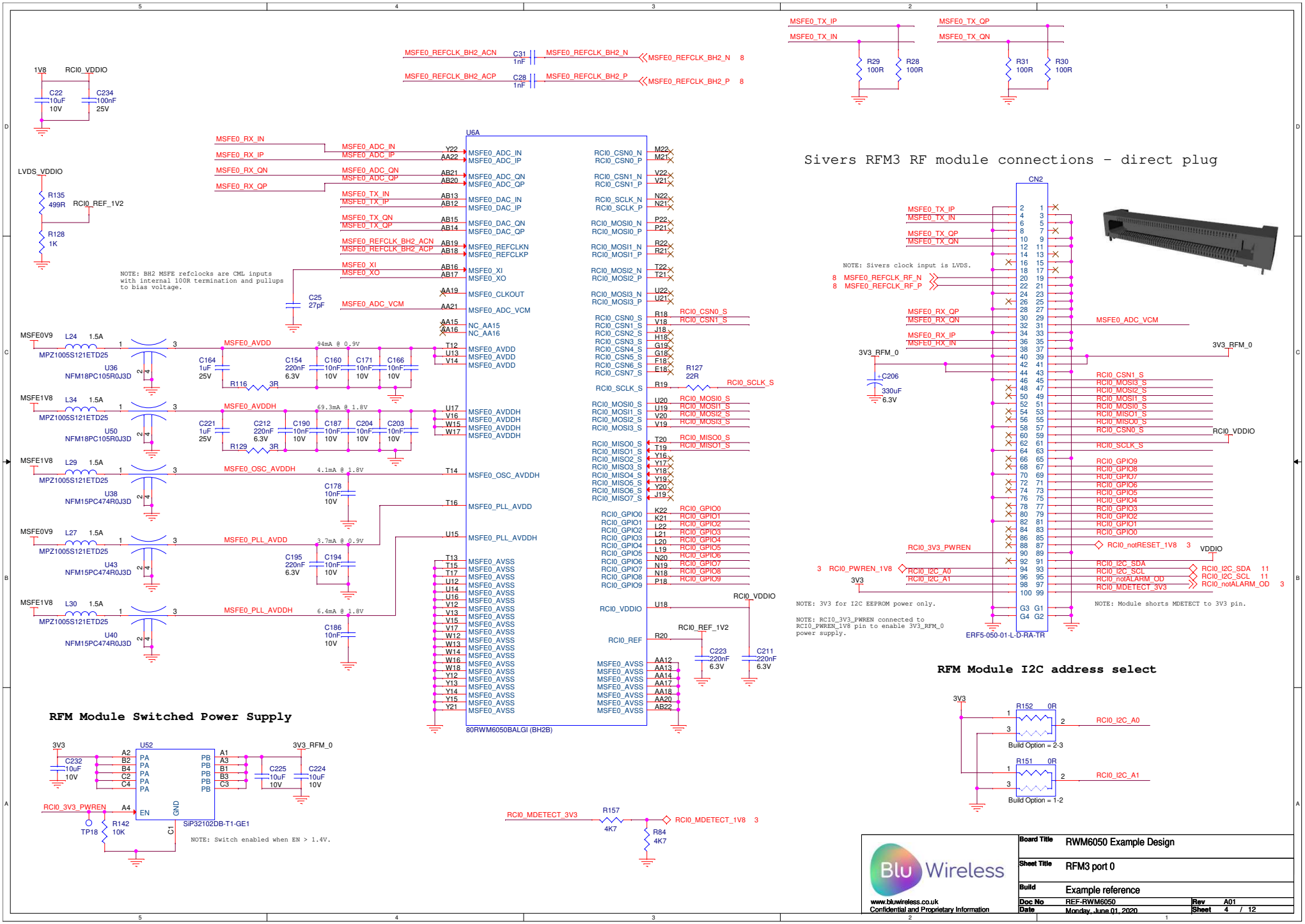
MSFE0_REFCLK_BH2_ACN
C31 1nF
MSFE0_REFCLK_BH2_N
MSFE0_REFCLK_BH2_N 8
MSFE0_REFCLK_BH2_ACP
C28 1nF
MSFE0_REFCLK_BH2_P
MSFE0_REFCLK_BH2_P 8
MSFE0_TX_IP
MSFE0_TX_IN
MSFE0_TX_QP
MSFE0_TX_QN
R29 100R
R28 100R
R31 100R
R30 100R
1V8
RCI0_VDDIO
C22 10uF 10V
C234 100nF 25V
LVDS_VDDIO
R135 499R
RCI0_REF_1V2
R128 1K
U6A
MSFE0_RX_IN
MSFE0_RX_IP
MSFE0_RX_QN
MSFE0_RX_QP
MSFE0_ADC_IN
MSFE0_ADC_IP
MSFE0_ADC_QN
MSFE0_ADC_QP
MSFE0_TX_IN
MSFE0_TX_IP
MSFE0_TX_QN
MSFE0_TX_QP
MSFE0_REFCLK_BH2_ACN
MSFE0_REFCLK_BH2_ACP
MSFE0_XI
MSFE0_XO
MSFE0_CLKOUT
MSFE0_ADC_VCM
NC_AA15
NC_AA16
MSFE0_DAC_IN
MSFE0_DAC_IP
MSFE0_DAC_QN
MSFE0_DAC_QP
MSFE0_REFCLKN
MSFE0_REFCLKP
NOTE: BH2 MSFE refclocks are CML inputs with internal 100R termination and pullups to bias voltage.
C25 27pF
RCI0_CSN0_N
RCI0_CSN0_P
RCI0_CSN1_N
RCI0_CSN1_P
RCI0_SCLK_N
RCI0_SCLK_P
RCI0_MOSI0_N
RCI0_MOSI0_P
RCI0_MOSI1_N
RCI0_MOSI1_P
RCI0_MOSI2_N
RCI0_MOSI2_P
RCI0_MOSI3_N
RCI0_MOSI3_P
RCI0_CSN0_S
RCI0_CSN1_S
RCI0_CSN2_S
RCI0_CSN3_S
RCI0_CSN4_S
RCI0_CSN5_S
RCI0_CSN6_S
RCI0_CSN7_S
R127 22R
RCI0_SCLK_S
RCI0_MOSI0_S
RCI0_MOSI1_S
RCI0_MOSI2_S
RCI0_MOSI3_S
RCI0_MISO0_S
RCI0_MISO1_S
RCI0_MISO2_S
RCI0_MISO3_S
RCI0_MISO4_S
RCI0_MISO5_S
RCI0_MISO6_S
RCI0_MISO7_S
RCI0_GPIO0
RCI0_GPIO1
RCI0_GPIO2
RCI0_GPIO3
RCI0_GPIO4
RCI0_GPIO5
RCI0_GPIO6
RCI0_GPIO7
RCI0_GPIO8
RCI0_GPIO9
RCI0_VDDIO
RCI0_REF
RCI0_REF_1V2
R20
C223 220nF 6.3V
C211 220nF 6.3V
MSFE0V9
L24 1.5A
MPZ1005S121ETD25
U36
NFM18PC105R0J3D
MSFE0_AVDD
94mA @ 0.9V
C164 1uF 25V
C154 220nF 6.3V
C160 10nF 10V
C171 10nF 10V
C166 10nF 10V
R116 3R
MSFE1V8
L34 1.5A
U50
MSFE0_AVDDH
69.3mA @ 1.8V
C221 1uF 25V
C212 220nF 6.3V
C190 10nF 10V
C187 10nF 10V
C204 10nF 10V
C203 10nF 10V
R129 3R
L29 1.5A
U38
NFM15PC474R0J3D
MSFE0_OSC_AVDDH
4.1mA @ 1.8V
C178 10nF 10V
MSFE0_PLL_AVDD
L27 1.5A
U43
3.7mA @ 0.9V
C195 220nF 6.3V
C194 10nF 10V
L30 1.5A
U40
6.4mA @ 1.8V
C186 10nF 10V
MSFE0_AVSS
80RWM6050BALGI (BH2B)
Sivers RFM3 RF module connections - direct plug
CN2
NOTE: Sivers clock input is LVDS.
8 MSFE0_REFCLK_RF_N
8 MSFE0_REFCLK_RF_P
3V3_RFM_0
C206 330uF 6.3V
ERF5-050-01-L-D-RA-TR
NOTE: 3V3 for I2C EEPROM power only.
NOTE: RCI0_3V3_PWREN connected to RCI0_PWREN_1V8 pin to enable 3V3_RFM_0 power supply.
RCI0_3V3_PWREN
3 RCI0_PWREN_1V8
RCI0_I2C_A0
RCI0_I2C_A1
RCI0_I2C_SDA 11
RCI0_I2C_SCL 11
RCI0_notALARM_OD 3
RCI0_MDETECT_3V3
RCI0_notRESET_1V8 3
NOTE: Module shorts MDETECT to 3V3 pin.
RFM Module Switched Power Supply
3V3
U52
C232 10uF 10V
3V3_RFM_0
C225 10uF 10V
C224 10uF 10V
RCI0_3V3_PWREN
R142 10K
TP18
SiP32102DB-T1-GE1
NOTE: Switch enabled when EN > 1.4V.
RCI0_MDETECT_3V3
R157 4K7
R84 4K7
RCI0_MDETECT_1V8 3
RFM Module I2C address select
R152 0R
Build Option = 2-3
R151 0R
Build Option = 1-2
RCI0_I2C_A0
RCI0_I2C_A1
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Sheet Title RFM3 port 0
Build Example reference
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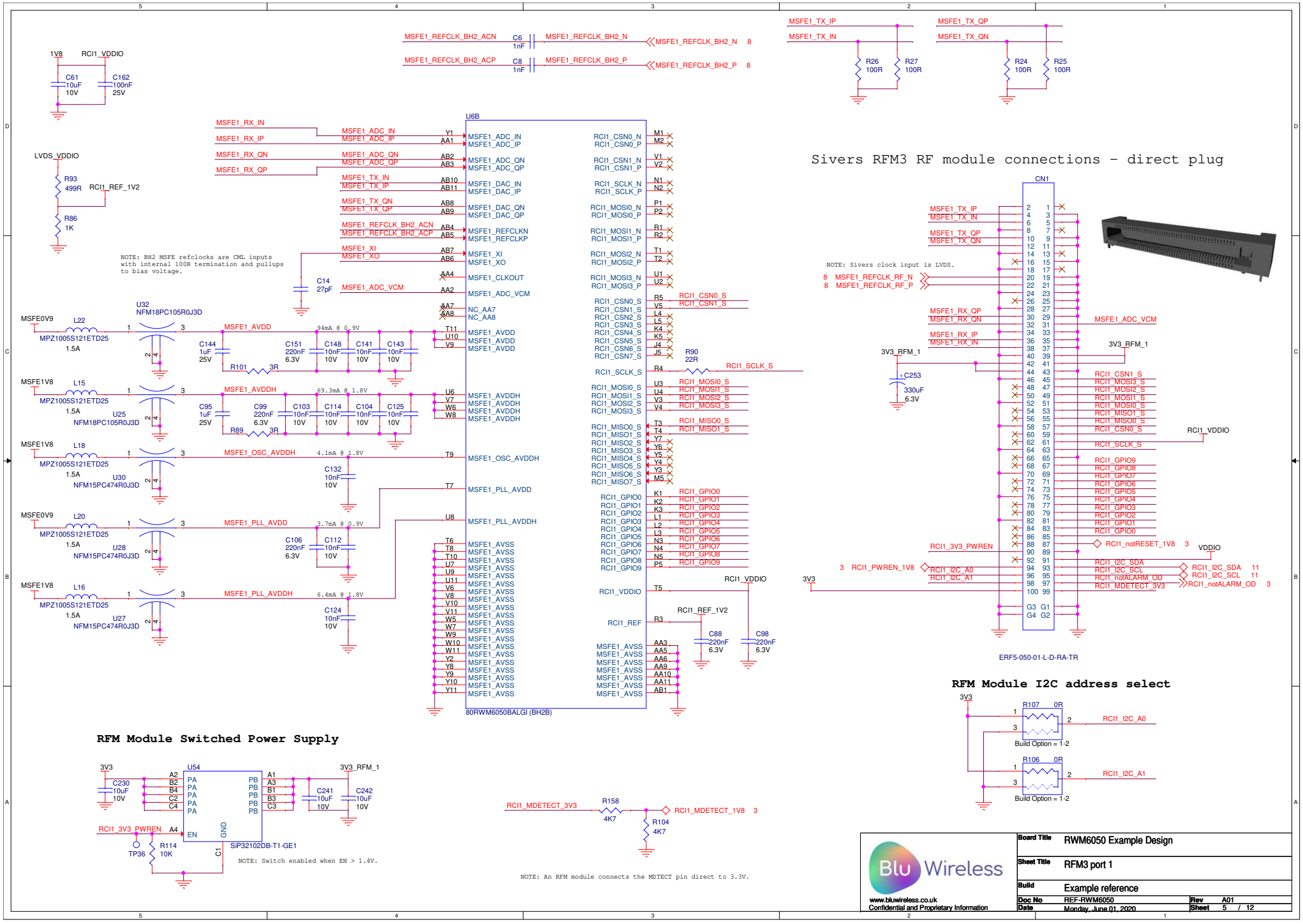
Sivers RFM3 RF module connections – direct plug
RFM Module Switched Power Supply
RFM Module I2C address select
U6B
80RWM6050BALGI (BH2B)
CN1
ERF5-050-01-L-D-RA-TR
U54
SiP32102DB-T1-GE1
NOTE: BH2 MSFE refclocks are CML inputs with internal 100R termination and pullups to bias voltage.
NOTE: Sivers clock input is LVDS.
NOTE: Switch enabled when EN > 1.4V.
NOTE: An RFM module connects the MDTECT pin direct to 3.3V.
Build Option = 1-2
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Board Title RWM6050 Example Design
Sheet Title RFM3 port 1
Build Example reference
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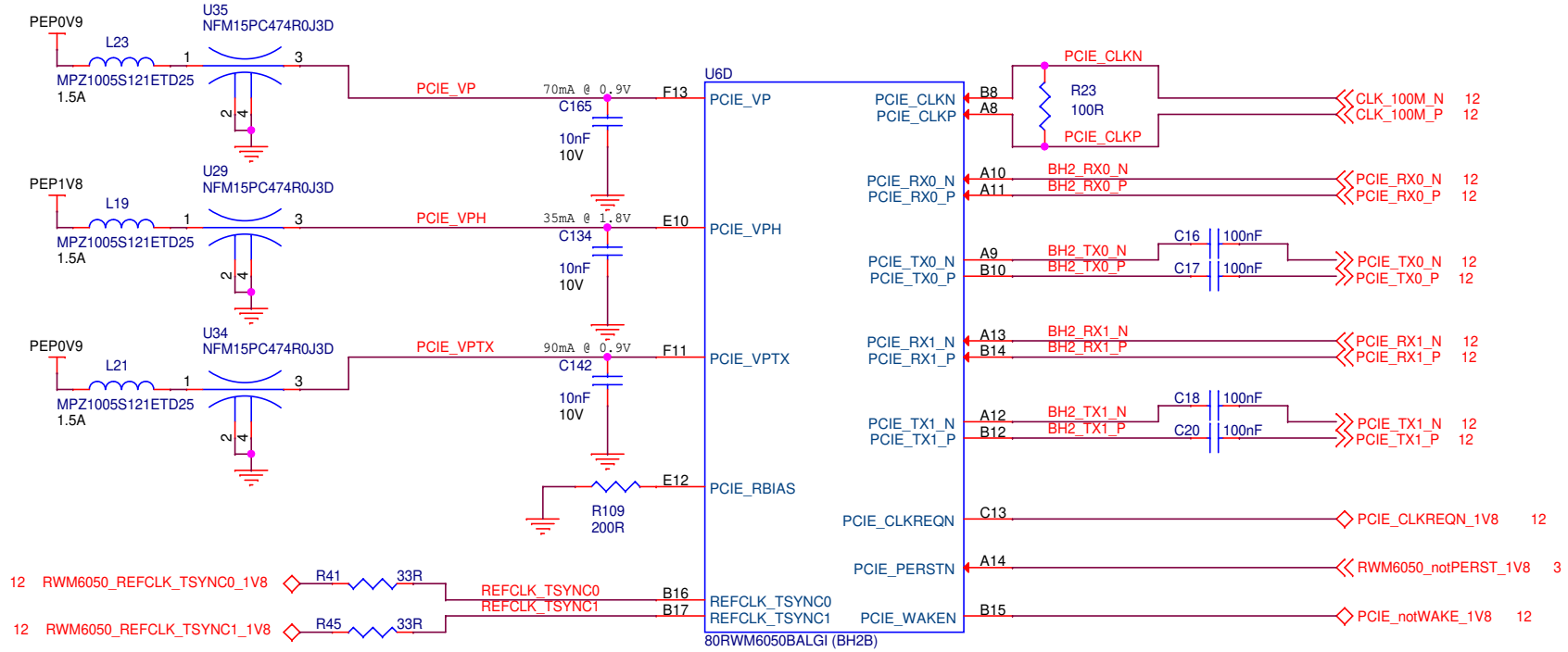
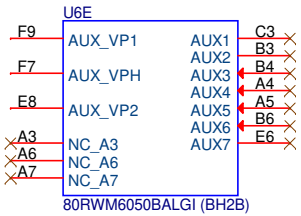


TSYNC0 and TSYNC1 should be length matched

TSYNC0 = IEEE1588v2 50/100MHz reference clock.
TSYNC1 = IEEE1588v2 1PPS time reference.

Unused pins



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Board Title	RWM6050 Example Design
Sheet Title	RWM6050 PCIe
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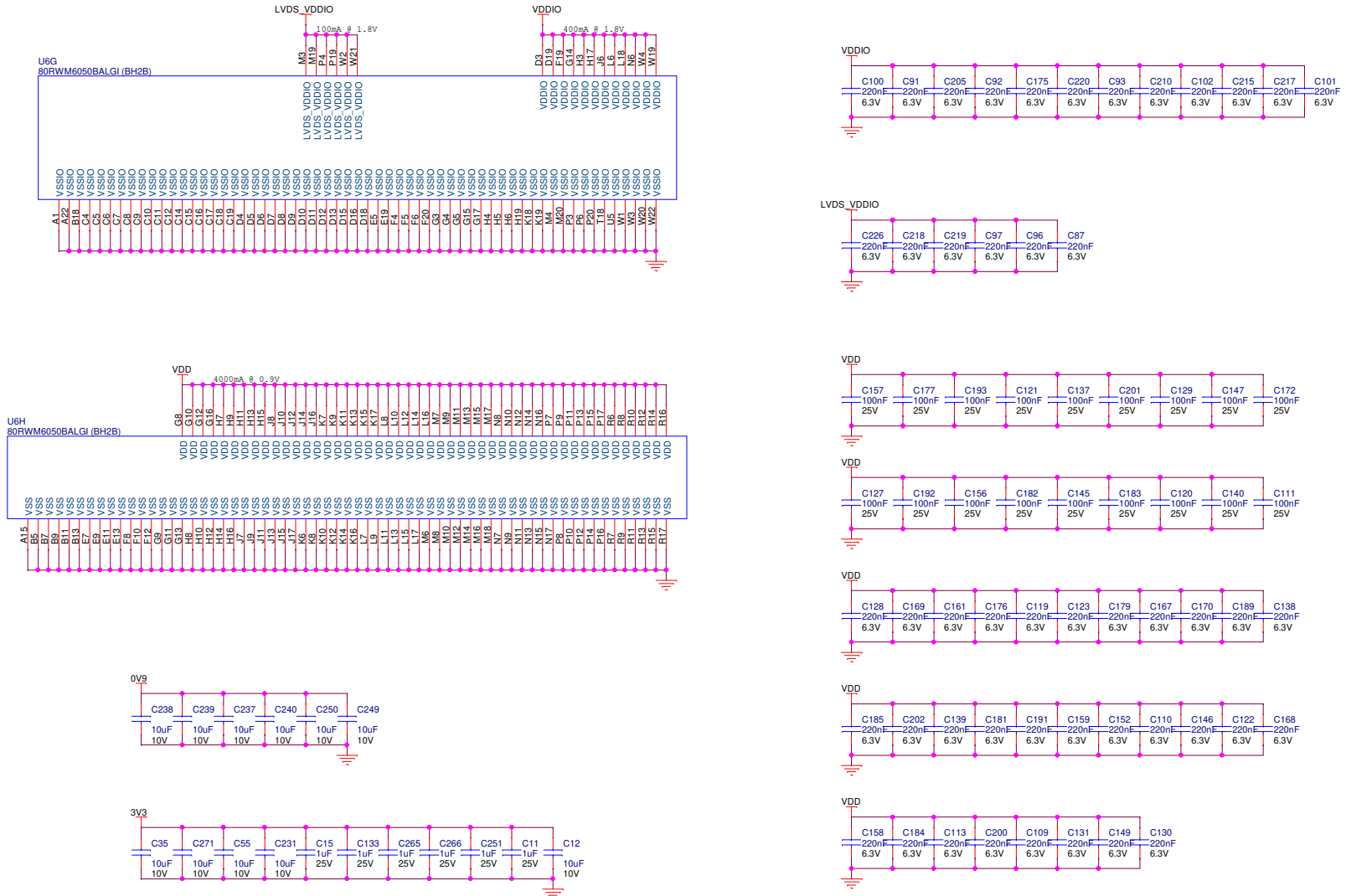

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Board Title	RWM6050 Example Design
Sheet Title	RWM6050 power
Build	Example reference
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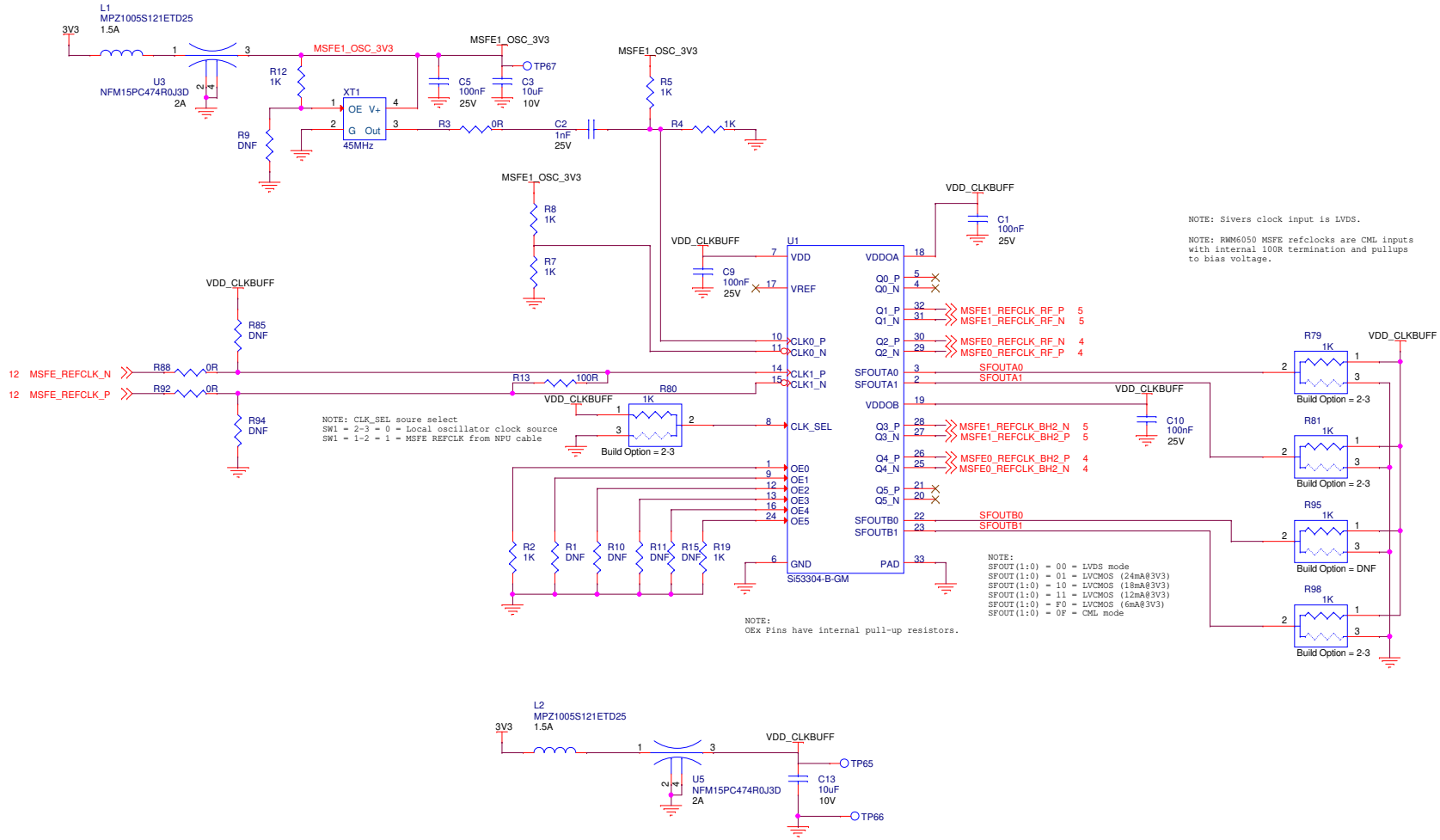

Board Title	RWM6050 Example Design
Sheet Title	MSFE Clock distribution
Build	Example reference
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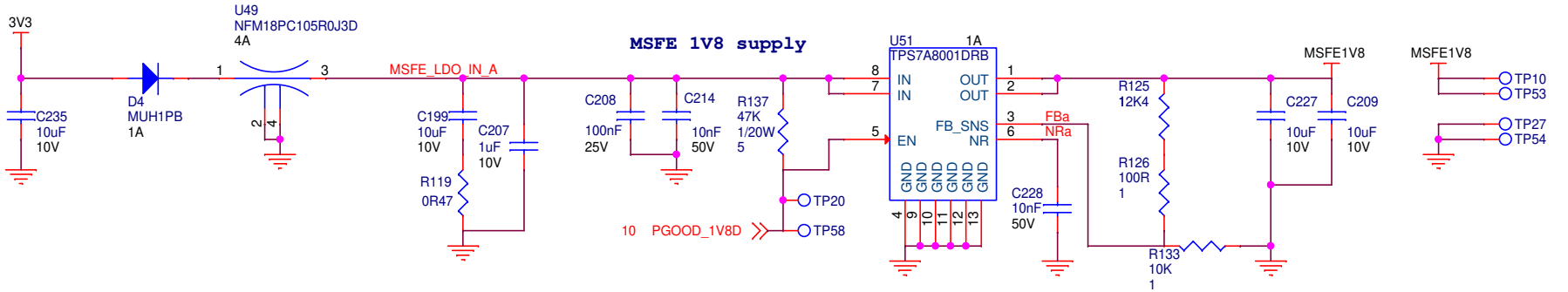
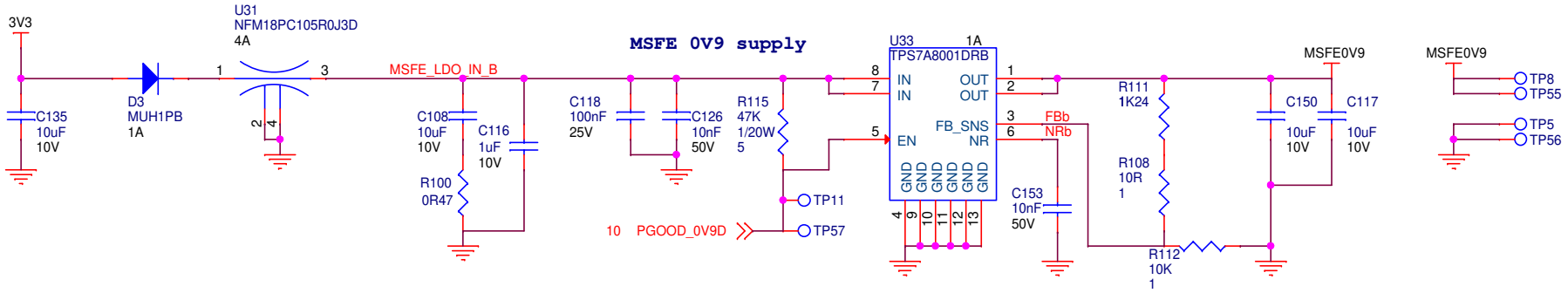
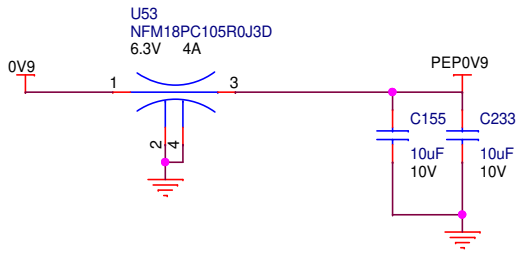




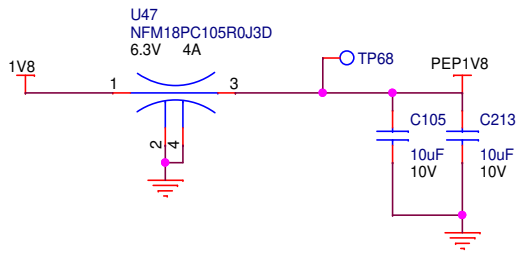
NOTE: MSFE recommended power seqence:
1) AVDD_H (1V8)
2) DVDD (0V9)
3) AVDD (0V9)

NOTE: LDO enabled when EN > 1.2V when 2.2V < VIN < 3.6V

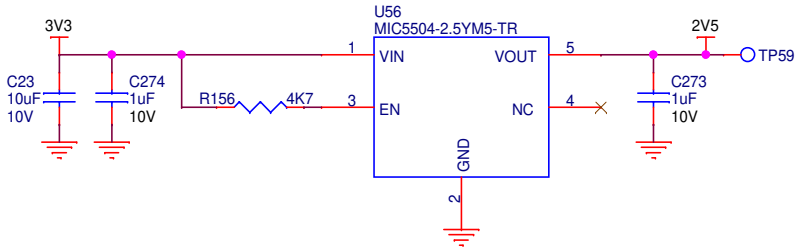
PCIe/Ethernet/PLL 0V9 supply



PCIe/PLL 1V8 supply



I2C 2V5 supply



Board Title	RWM6050 Example Design
Sheet Title	Analog power supplies
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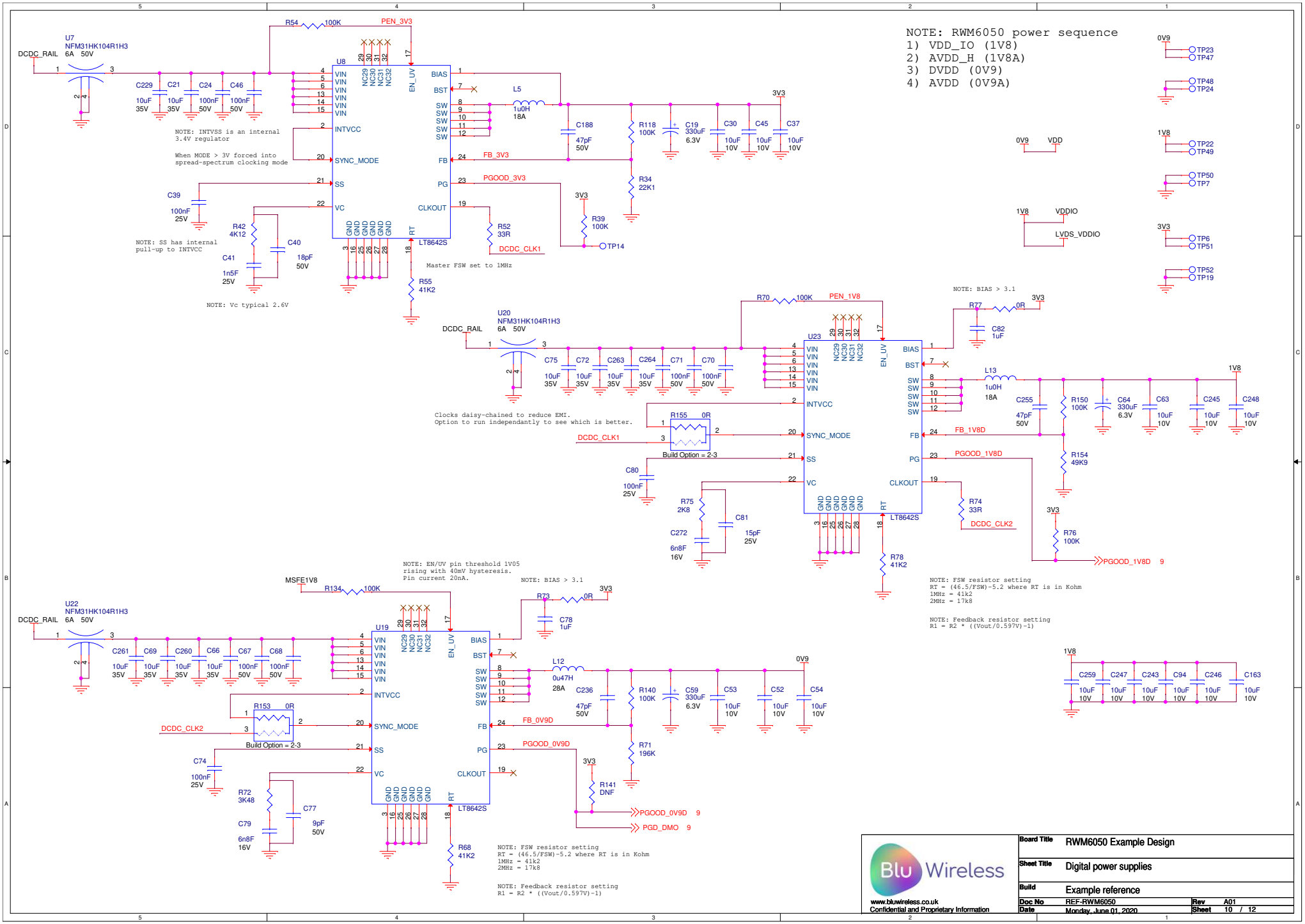
NOTE: RWM6050 power sequence
1) VDD_IO (1V8)
2) AVDD_H (1V8A)
3) DVDD (0V9)
4) AVDD (0V9A)
U7
NFM31HK104R1H3
DCDC_RAIL 6A 50V
R54 100K
PEN_3V3
U8
LT8642S
NOTE: INTVSS is an internal 3.4V regulator
When MODE > 3V forced into spread-spectrum clocking mode
NOTE: SS has internal pull-up to INTVCC
NOTE: Vc typical 2.6V
Master FSW set to 1MHz
FB_3V3
PGOOD_3V3
DCDC_CLK1
L5 1u0H 18A
R118 100K
R34 22K1
R39 100K
TP14
R52 33R
R55 41K2
U20
NFM31HK104R1H3
DCDC_RAIL 6A 50V
R70 100K
PEN_1V8
U23
LT8642S
Clocks daisy-chained to reduce EMI.
Option to run independantly to see which is better.
R155 0R
Build Option = 2-3
DCDC_CLK1
FB_1V8D
PGOOD_1V8D
L13 1u0H 18A
R154 49K9
R74 33R
DCDC_CLK2
R76 100K
R78 41K2
NOTE: BIAS > 3.1
NOTE: FSW resistor setting
RT = (46.5/FSW)-5.2 where RT is in Kohm
1MHz = 41k2
2MHz = 17k8
NOTE: Feedback resistor setting
R1 = R2 * ((Vout/0.597V)-1)
U22
NFM31HK104R1H3
DCDC_RAIL 6A 50V
MSFE1V8
R134 100K
U19
LT8642S
NOTE: EN/UV pin threshold 1V05 rising with 40mV hysteresis.
Pin current 20nA.
R153 0R
Build Option = 2-3
DCDC_CLK2
FB_0V9D
PGOOD_0V9D
L12 0u47H 28A
R71 196K
R141 DNF
PGD_DMO
R68 41K2
NOTE: FSW resistor setting
RT = (46.5/FSW)-5.2 where RT is in Kohm
1MHz = 41k2
2MHz = 17k8
NOTE: Feedback resistor setting
R1 = R2 * ((Vout/0.597V)-1)
0V9
VDD
1V8
VDDIO
LVDS_VDDIO
3V3
TP23
TP47
TP48
TP24
TP22
TP49
TP50
TP7
TP6
TP51
TP52
TP19
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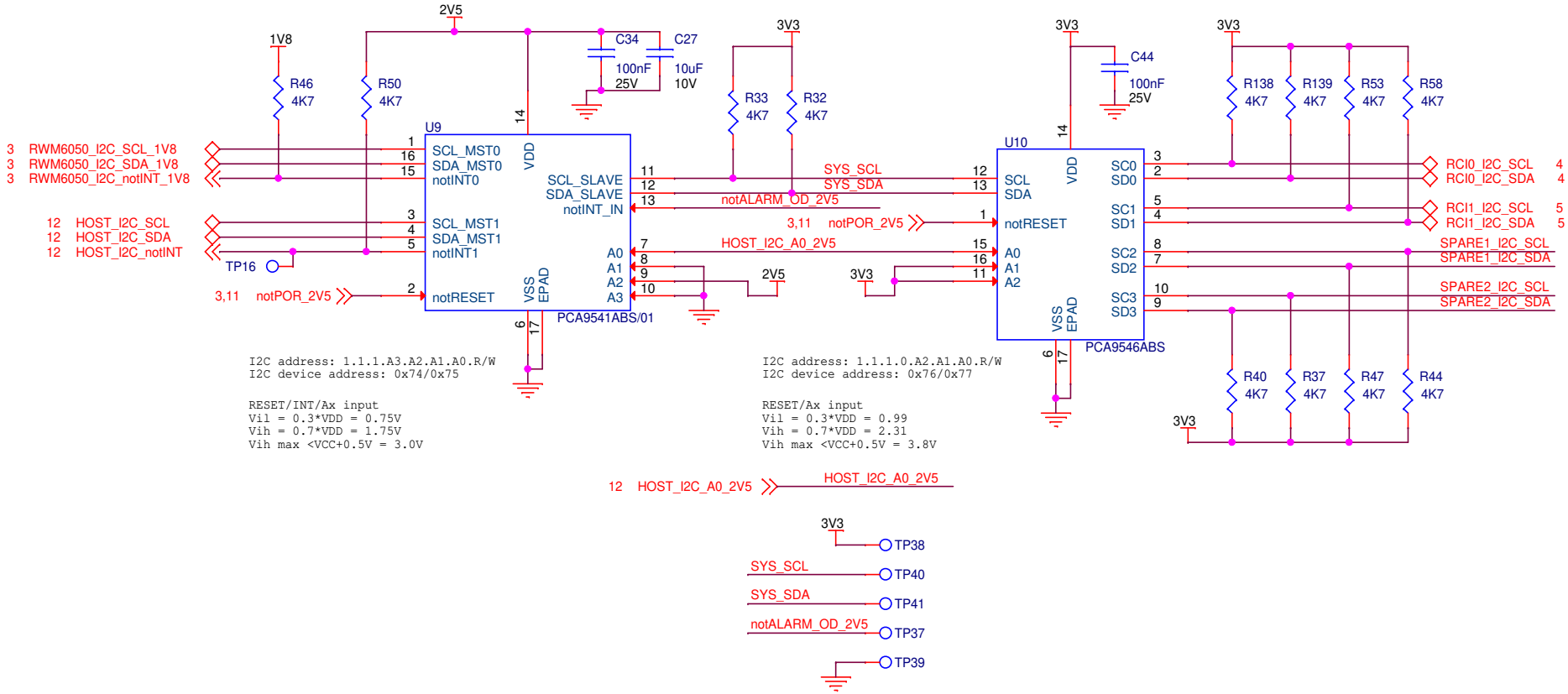
I2C Arbiter and hub



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Front end to back end connections

This page is used to connect the RWM6050 front end to the down stream interface.
When connecting to a down stream service, take care to ensure that the signals are the relevant voltage level.

Signals from BH2 **Signals from NPU**

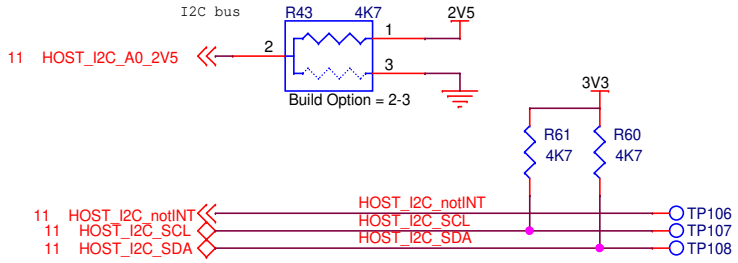
System signals

MRESET triggers the POR circuitry.

3 HOST_notMRESET — HOST_notMRESET — TP86

SYSRESET connects to the RWM6050 system and PERST resets.

3 HOST_notSYSRESET — HOST_notPERST — TP87



RWM6050 Boot flash programming interface

FSPI_PROG_EN — HOST_PROG_EN — TP88
FSPI_PROG_CSN — HOST_SPI_CSN — TP89
FSPI_PROG_CLK — HOST_SPI_CLK — TP90
FSPI_PROG_MISO — HOST_SPI_MISO — TP91
FSPI_PROG_MOSI — HOST_SPI_MOSI — TP92
FSPI_PROG_notHOLD — HOST_SPI_notHOLD — TP93
FSPI_PROG_notWP — HOST_SPI_notWP — TP94

Debug signals

3 RWM6050_UART_RX_1V8 — HOST_UART_RX — TP95
3 RWM6050_UART_TX_1V8 — HOST_UART_TX — TP96

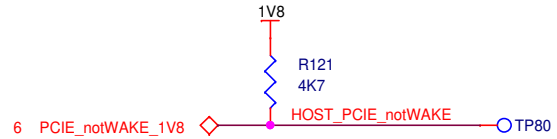
GPIO signals

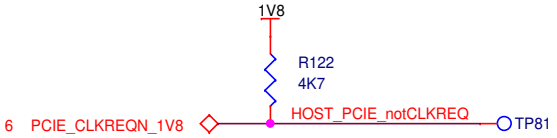
3 EXP_GPIO7_1V8 — TP104
3 EXP_GPIO6_1V8 — TP103
3 EXP_GPIO5_1V8 — TP9
3 EXP_GPIO4_1V8 — TP105
3 EXP_GPIO3_1V8 — TP1
3 EXP_GPIO2_1V8 — TP2
3 EXP_GPIO1_1V8 — TP3
3 EXP_GPIO0_1V8 — TP4

PCIe signals

Signals from/to RWM6050 **Signals to/from HOST**

6 CLK_100M_N — PCIe_CLK_100M_N — TP70
6 CLK_100M_P — PCIe_CLK_100M_P — TP71
6 PCIE_TX0_N — HOST_PCIE_RX0_N — TP72
6 PCIE_TX0_P — HOST_PCIE_RX0_P — TP73
6 PCIE_RX0_N — HOST_PCIE_TX0_N — TP74
6 PCIE_RX0_P — HOST_PCIE_TX0_P — TP75
6 PCIE_TX1_N — HOST_PCIE_RX1_N — TP76
6 PCIE_TX1_P — HOST_PCIE_RX1_P — TP77
6 PCIE_RX1_N — HOST_PCIE_TX1_N — TP78
6 PCIE_RX1_P — HOST_PCIE_TX1_P — TP79





IEEE1588 signals

6 RWM6050_REFCLK_TSYNC0_1V8 — HOST_TSU_CLK — TP82
6 RWM6050_REFCLK_TSYNC1_1V8 — HOST_TSU_SYNC — TP83
8 MSFE_REFCLK_N — HOST_MSFE_REFCLK_N — TP84
8 MSFE_REFCLK_P — HOST_MSFE_REFCLK_P — TP85

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