Tsi577™ Device Errata

Formal Status

July 11, 2014

About this Document

Revision History

July 11, 2014, Formal

Updated the second work around in [DEV4] Clock compensation sequence missing during link initialization

May 9, 2013, Formal

Added a new erratum, [DEV4] Clock compensation sequence missing during link initialization

July 17, 2012, Formal

Removed the confidential statement from the document's footers

April 1, 2010, Formal

- Added the following erratum: [DEV3] Lookup table routing issue
- Updated the following errata:
  - [DEV1] Align character inserted into KRRR sequence
  - [DEV2] 4x port in 1x mode transmission on lane 0 and lane 2 issue
  - [ERR1] Disabling port with OUTPUT_EN may cause incorrect packets to be sent

August 2009, Formal

This document was updated to reflect IDT. There were no technical changes.

January 2009, Formal

This is the first release of the *Tsi577 Device Errata*.

1. Device Errata

Errata Name
Device
[DEV1] Align character inserted into KRRR sequence
[DEV2] 4x port in 1x mode transmission on lane 0 and lane 2 issue
[DEV3] Lookup table routing issue
[DEV4] Clock compensation sequence missing during link initialization
Error Handling
[ERR1] Disabling port with OUTPUT_EN may cause incorrect packets to be sent
[ERR2] Switch Time-to-Live (TTL) not supported

[DEV1] Align character inserted into KRRR sequence

Description

The Tsi577 embeds an align character (/A/ or ||A||) within the idle sequence at intervals required by the *RapidIO Interconnect Specification (Revision 1.3)*. There is a small probability that this align character will be embedded within the clock compensation sequence (KRRR), resulting in a RapidIO non-compliance. The RapidIO Specification requires a device to send a clock compensation sequence at least once every 5000 characters on each lane.

Impact

The probability of multiple corrupt clock compensation sequences is very small, and most members of the RapidIO ecosystem have a robust design, so it is unlikely that this issue will have a measurable impact. Multiple corrupt clock compensation sequences could cause the detection of a transmission error by the link partner if the transmitter is operating at a clock rate faster than the receiver, as allowed by the RapidIO Specification.

Work Around

None.

[DEV2] 4x port in 1x mode transmission on lane 0 and lane 2 issue

Description

The *RapidIO Interconnect Specification (Revision 1.3)* for a 4x link operating in 1x mode states the following:

> A 4x port operating in 1x mode shall encode and transmit the character stream of delimited control symbols and packets received from the upper layers over both lanes 0 and 2 in the order the characters were received from the upper layers.

When a Tsi577 4x port is operating in 1x redundancy mode as described above, the Tsi577 transmits on one lane only instead of the behavior described in the RapidIO Specification.

Impact

The Tsi577 may be unable to establish communication in the event of a hardware fault due to this non-compliance with this aspect of the RapidIO Specification.

Work Around

None.

[DEV3] Lookup table routing issue

Description

The following example will help explain the issue. A system with Device X is connected to Port A of a Tsi577 switch, and Device Y is connected to Port B of the same switch. When Device X reads the registers in Port A while Device Y also reads an entry from Port A's local LUT, there is a two register bus clock cycle window whereby Device Y may receive incorrect data.

This situation occurs when Port A is Port 0 and Device Y reads the value of the global LUT from the RapidIO standard registers (offset 0x70/0x74), or from the Tsi577 implementation-specific registers (offset 0x10070/10074), since reads of the global LUT use Port 0's local LUT.

This situation also occurs when Port A is not port 0, and Device Y reads from Port A's local LUT.

Impact

Software will operate with incorrect routing table data.

Work Arounds

Either of the following work arounds can be implemented:

1. When reading LUT values, always read from the port on the switch that the endpoint is connected to. If Device Y always reads LUT values from the local LUT of Port B, it will always receive correct data.
2. Alternatively, read the LUT entry multiple times. Choose the value that was returned most often.

[DEV4] Clock compensation sequence missing during link initialization

Description

During link initialization the Tsi577 does not send clock compensation sequences after 4096 S_CLK clock periods.

Impact

This issue may cause protocol errors during link initialization depending on the difference in the reference clock frequency between the Tsi577 and its link partner. Devices that check for the presence of clock compensation sequences may not successfully initialize the link with the Tsi577. These devices include the following Gen2 Revision C switches: CPS-1848 and CPS-1432.

Work Arounds

Either of the following work arounds can be implemented:

1. If the port is initially configured as a x4 link but only a x1 link is required then system software can force a downgrade by using the Override Port Width capability. To do so, set the Tsi577's SP{0..15}_CTL [OVER_PWIDTH] to the desired 1x lane.
2. Disable checking for clock compensation sequences by the link partner. For the CPS-1848 and CPS-1432 devices this can be accomplished by setting LANE_n_STATUS_4_CSR[CC_MONITOR_EN] to 0 for the affected lanes. If this link may be hot swapped then set CC_MONITOR_EN back to 1 after PORT_OK has been achieved. This will enable detection of the hot swap event.

[ERR1] Disabling port with OUTPUT_EN may cause incorrect packets to be sent

Description

If the following conditions occur concurrently, an end of packet (EOP) control symbol for the packet may not be sent to the physical layer:

- A port is disabled on the Tsi577 by clearing the port's OUTPUT_EN bit in the Serial Port Control CSR
- The port's output buffer receives the last datum of a packet from the ISF
- The physical layer is transmitting the packet to the link partner

This causes the physical layer to send contiguous status controls symbols until the next maintenance packet is sent to the output buffer. Receiving a maintenance packet causes a packet not accepted (PNA) control symbol to be sent. The link then performs error recovery.

Impact

When the Tsi577 is in this state, it cannot send the clock compensation pattern required by the *RapidIO Interconnect Specification (Revision 1.3)*.

Work Around

In order to avoid experiencing this erratum, change all routing tables to discard packets sent to the port about to be disabled before clearing the OUTPUT_EN bit. To recover from this event, reset the port.

[ERR2] Switch Time-to-Live (TTL) not supported

Description

The Tsi577 does not support Time-to-Live functionality required for a switch in the *RapidIO Interconnect Specification (Revision 1.3)*, *RapidIO Error Management Extensions*.

Work Around

None.

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