Tsi578™ Device Errata

Formal Status

July 11, 2014

About this Document

This document discusses device errata for the Tsi578.

Revision History

July 11, 2014, Formal

Updated the second work around in [DEV5] Clock compensation sequence missing during link initialization

May 9, 2013, Formal

Added a new erratum, [DEV5] Clock compensation sequence missing during link initialization.

July 17, 2012, Formal

Removed the confidential statement from the document's footers.

April 1, 2010, Formal

- Added the following erratum: [DEV4] Lookup table routing issue
- Updated the following errata:
    — [DEV2] Align character inserted into KRRR sequence
    — [DEV3] 4x port in 1x mode transmission on lane 0 and lane 2 issue
    — [ERR2] Disabling port with OUTPUT_EN may cause incorrect packets to be sent

July 24, 2009, Formal

This document was updated with IDT formatting. There were no technical changes.

January 2009, Formal

Added the following errata:

- [REG6] Logical layer error capture registers may not capture errors
- [ERR4] Switch Time-to-Live not supported

May 2008, Formal

The following errata were added:

- [REG5] Host Base Device ID register locks with 0xFFFF
- [ERR3] Exceeding error threshold limit

February 2008, Formal

Multiple titles have been changed throughout the document in an attempt to clarify the errata. All of the errata represent the production version of the device. The following errata were added or clarified:

- [REG3] Address not captured for invalid maintenance packet
- [REG4] Performance statistics counter outbound measurement
- [ERR2] Disabling port with OUTPUT_EN may cause incorrect packets to be sent

1. Device Errata

Errata Name
Device
[DEV1] Multicast control symbol loss
[DEV2] Align character inserted into KRRR sequence
[DEV3] 4x port in 1x mode transmission on lane 0 and lane 2 issue
[DEV4] Lookup table routing issue
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Registers
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[ERR3] Exceeding error threshold limit
[ERR4] Switch Time-to-Live not supported

[DEV1] Multicast control symbol loss

Description

Multicast control symbols (MCES) are not reliably transmitted, or re-transmitted, if they are generated for transmission concurrent with the transmission of a start-of-packet control symbol.

This issue can occur when an MCES is triggered in the following ways:

- Transition of the MCES pin
- Reception of an MCES on a link (re-transmission required)
- Software

> Multicast control symbols are used in a system to transmit heart beat information to synchronize endpoints and are, generally, sent at the same time traffic is being transmitted.

The following examples show how this errata can be triggered.

Example One

If the MCES is queued for transmission at the same time as a packet delimiter, the multicast control symbol is not transmitted.

Example Two

If packets are being transmitted on a link back-to-back at the line rate of the port there is a possibility that an MCES will be transmitted twice.

A port is required to send a status control symbol at least once every 5000 characters transmitted on the link. When packets are being transmitted back-to-back at line rate and a Status control symbol and an MCES are queued up concurrently, the Status control symbol will not be transmitted and, instead, the MCES will be transmitted. This results in two MCES being transmitted for one MCES stimulus.

Impact

In a worst-case situation, the Tsi578 would lose, on average, 33 per cent of multicast controls symbols.

Work Around

None.

[DEV2] Align character inserted into KRRR sequence

Description

The Tsi578 embeds an align character (/A/ or ||A||) within the idle sequence at intervals required by the *RapidIO Interconnect Specification (Revision 1.3)*. There is a small probability that this align character will be embedded within the clock compensation sequence (KRRR), resulting in a RapidIO non-compliance. The RapidIO Specification requires a device to send a clock compensation sequence at least once every 5000 characters on each lane.

Impact

The probability of multiple corrupt clock compensation sequences is very small, and most members of the RapidIO ecosystem have a robust design, so it is unlikely that this issue will have a measurable impact. Multiple corrupt clock compensation sequences could cause the detection of a transmission error by the link partner if the transmitter is operating at a clock rate faster than the receiver, as allowed by the RapidIO Specification.

Work Around

None.

[DEV3] 4x port in 1x mode transmission on lane 0 and lane 2 issue

Description

The *RapidIO Interconnect Specification (Revision 1.3)* for a 4x link operating in 1x mode states the following:

A 4x port operating in 1x mode shall encode and transmit the character stream of delimited control symbols and packets received from the upper layers over both lanes 0 and 2 in the order the characters were received from the upper layers.

When a Tsi578 4x port is operating in 1x redundancy mode as described above, the Tsi578 transmits on one lane only instead of the behavior described in the RapidIO Specification.

Impact

The Tsi578 may be unable to establish communication in the event of a hardware fault due to this non-compliance with this aspect of the RapidIO Specification.

Work Around

None.

[DEV4] Lookup table routing issue

Description

The following example will help explain the issue. A system with Device X is connected to Port A of a Tsi578 switch, and Device Y is connected to Port B of the same switch. When Device X reads the registers in Port A while Device Y also reads an entry from Port A's local LUT, there is a two register bus clock cycle window whereby Device Y may receive incorrect data.

This situation occurs when Port A is Port 0 and Device Y reads the value of the global LUT from the RapidIO standard registers (offset 0x70/0x74), or from the Tsi578 implementation-specific registers (offset 0x10070/10074), since reads of the global LUT use Port 0's local LUT.

This situation also occurs when Port A is not port 0, and Device Y reads from Port A's local LUT.

Impact

Software will operate with incorrect routing table data.

Work Around

Either of the following work arounds can be implemented:

1. When reading LUT values, always read from the port on the switch that the endpoint is connected to. If Device Y always reads LUT values from the local LUT of Port B, it will always receive correct data.

2. Alternatively, read the LUT entry multiple times. Choose the value that was returned most often.

[DEV5] Clock compensation sequence missing during link initialization

Description

During link initialization the Tsi578 does not send clock compensation sequences after 4096 S_CLK clock periods.

Impact

This issue may cause protocol errors during link initialization depending on the difference in the reference clock frequency between the Tsi578 and its link partner. Devices that check for the presence of clock compensation sequences may not successfully initialize the link with the Tsi578. These devices include the following Gen2 Revision C switches: CPS-1848 and CPS-1432.

Work Arounds

Either of the following work arounds can be implemented:

1. If the port is initially configured as a x4 link but only a x1 link is required then system software can force a downgrade by using the Override Port Width capability. To do so, set the Tsi578's SP{0..15}_CTL [OVER_PWIDTH] to the desired 1x lane.

2. Disable checking for clock compensation sequences by the link partner. For the CPS-1848 and CPS-1432 devices, this can be accomplished by setting LANE_n_STATUS_4_CSR[CC_MONITOR_EN] to 0 for the affected lanes. If this link may be hot swapped then set CC_MONITOR_EN back to 1 after PORT_OK has been achieved. This will enable detection of the hot swap event.

[REG1] Register read race condition

Description

Reading specific registers in the Tsi578 may result in an incorrect value being read back due to a race condition in the read logic. The affected registers are shown in the following table.

Register Name	Register Offset
SMAC{0,2,4,6,8,10,12,14}_CFG_CH0	130B0, 132B0, 134B0, 136B0, 138B0, 13AB0, 13CB0, 13EB0
SMAC{0,2,4,6,8,10,12,14}_CFG_CH1	130B4, 132B4, 134B4, 136B4, 138B4, 13AB4, 13CB4, 13EB4
SMAC{0,2,4,6,8,10,12,14}_CFG_CH2	130B8, 132B8, 134B8, 136B8, 138B8, 13AB8, 13CB8, 13EB8
SMAC{0,2,4,6,8,10,12,14}_CFG_CH3	130BC, 132BC, 134BC, 136BC, 138BC, 13ABC, 13CBC, 13EBC
SMAC{0,2,4,6,8,10,12,14}_CFG_GBL	130C0, 132C0, 134C0, 136C0, 138C0, 13AC0, 13CC0, 13EC0
SMAC{0,2,4,6,8,10,12,14}_CFG_GBLB	130C4, 132C4, 134C4, 136C4, 138C4, 13AC4, 13CC4, 13EC4
SMAC{0,2,4,6,8,10,12,14}_PG_CTL_0	1E020, 1E220, 1E420, 1E620, 1E820, 1EA20, 1EC20, 1EE20
SMAC{0,2,4,6,8,10,12,14}_PG_CTL_1	1E060, 1E260, 1E460, 1E660, 1E860, 1E860, 1EC60, 1EE60
SMAC{0,2,4,6,8,10,12,14}_PG_CTL_2	1E0A0, 1E2A0, 1E4A0, 1E6A0, 1E8A0, 1EAA0, 1ECA0, 1EEA0
SMAC{0,2,4,6,8,10,12,14}_PG_CTL_3	1E0E0, 1E2E0, 1E4E0, 1E6E0, 1E8E0, 1EAE0, 1ECE0, 1EEE0
SMAC{0,2,4,6,8,10,12,14}_PM_CTL_0	1E030, 1E230, 1E430, 1E630, 1E830, 1EA30, 1EC30, 1EE30
SMAC{0,2,4,6,8,10,12,14}_PM_CTL_1	1E070, 1E270, 1E470, 1E670, 1E870, 1EA70, 1EC70, 1EE70
SMAC{0,2,4,6,8,10,12,14}_PM_CTL_2	1E0B0, 1E2B0, 1E4B0, 1E6B0, 1E8B0, 1EAB0, 1ECB0, 1EEB0
SMAC{0,2,4,6,8,10,12,14}_PM_CTL_3	1E0F0, 1E2F0, 1E4F0, 1E6F0, 1E8F0, 1EAF0, 1ECF0, 1EEF0
SMAC{0,2,4,6,8,10,12,14}_FP_VAL_0	1E034, 1E234, 1E434, 1E634, 1E834, 1EA24, 1EC24, 1EE24
SMAC{0,2,4,6,8,10,12,14}_FP_VAL_1	1E074, 1E274, 1E474, 1E674, 1E874, 1EA74, 1EC74, 1EE74
SMAC{0,2,4,6,8,10,12,14}_FP_VAL_2	1E0B4, 1E2B4, 1E4B4, 1E6B4, 1E8B4, 1EAB4, 1ECB4, 1EEB4
SMAC{0,2,4,6,8,10,12,14}_FP_VAL_3	1E0F4, 1E2F4, 1E4F4, 1E6F4, 1E8F4, 1EAF4, 1ECF4, 1EEF4

Impact

Writing to the registers is not affected.

Work Around

For non-dynamic bits, read the register multiple times and use the value which does not change.

[REG2] Lookup table parity data not logged

Description

When a LUT parity error occurs, information about the error is latched in the RIO Port x LUT Parity Error Info CSR. The PTY_BIT and LUT_VLD bits have an undefined value instead of the expected data from the LUT entry.

Impact

It is not possible to determine what bit in the LUT entry is incorrect.

Work Around

The LUT entry must be re-written with the correct value.

[REG3] Address not captured for invalid maintenance packet

When an incorrectly constructed maintenance packet (FTYPE = 8) with a Transport/Logical layer error is processed by the Tsi578, the Address field (ADDR) is not latched by the Logical and Transport layer Address Capture CSR (offset 0x1014). The Tsi578 does not capture the ADDR field for maintenance packets when one of the following errors occur:

- Illegal Transaction Type
- Illegal Transaction Type code
- Reserved Transaction Type
- Receive Port-write

Impact

Some information for diagnosis of an invalid maintenance packet is not available.

Work Around

None.

[REG4] Performance statistics counter outbound measurement

Description

The Performance Statistic Counters for a port can stop counting packet statistics for outbound traffic when retries are being received.

The following modes in the PSx_TYPE field in the RIO Port x Performance Statistics Counter N register are affected:

- 0b000 = Count all unicast request packets only. The response packets, maintenance packets, and maintenance packets with hop count of 0 are excluded from this counter.
- 0b001 = Count all unicast packet types. This counter includes all request, response, maintenance packets (including the maintenance packets with hop count 0).
- 0b100 = Count every 32-bits of unicast data. This counter counts all accepted unicast packets data (including header).
- 0b101= Count all multicast packets only.
- 0b111 = Count every 32-bits of multicast data. This counter includes counting the entire multicast packet (including header).

Impact

The statistics counters may not accurately reflect the outbound packet performance. When in this state, the counters return zero when packets are being successfully transferred.

Work Around

The following work arounds discuss what to do if the system encounters this issue, how to limit the impact in an already designed system, and how to design a system to avoid the issue.

Issue Encountered

If this issue is encountered, the port must be reset in order to restart the counter.

Limiting the Impact

Most RapidIO endpoints (for example, TI, Freescale, AMCC processors) are able to receive traffic at line rate. This means the Tsi578 should only see retries when there is an error. The outbound performance counters perform correctly until there is a retry.

If the Tsi578's link partner in the system is another Tsi57x switch, the data traffic being transmitted from a outbound Tsi578 port can be monitored by the link partner's inbound performance counters

The outbound performance counters are able to measure control symbol traffic. Information about the network could be inferred by measuring control symbols.

Avoiding the Issue Through System Design

The issue can be avoided by engineering the system traffic patterns to eliminate retries.

Also, if the design has an unused Tsi578 port, the port can be configured in Digital Loopback Mode and traffic can be routed to the port. This enables the inbound performance counters to gather performance statistics that are equivalent to the outbound performance.

[REG5] Host Base Device ID register locks with 0xFFFF

Description

Writing a value of 0xFFFF to the Host Base Device ID CSR (Offset 0x68) locks the register.

Impact

System software should not write a value of 0xFFFF in order to lock the register.

Work Around

System software should read back the value written into the Host Base Device ID CSR. If the read-back encounters 0xFFFF, then the register has been locked with 0xFFFF and must be unlocked by writing 0xFFFF. The register must then be re-written with the required value to re-lock the register.

[REG6] Logical layer error capture registers may not capture errors

Description

When port-writes are disabled (SPx_MODE[PW_DIS] = 1) in ports 1-X, and a logical layer error is detected on these ports, the logical layer error capture registers (RIO_LOG_ERR_ADDR, RIO_LOG_ERR_DEVID, and RIO_LOG_ERR_CTRL_INFO) do not capture the error.

Impact

Error diagnosis is impaired when port-writes are disabled.

Work Around

Enable port-writes.

[ERR1] Error rate counter limitation

Description

After an initial TEA or MC_TEA error, the ERR_RATE_CNT field in the Error Rate register does not count subsequent errors unless the OUTPUT_DROP status bit is toggled from 0 to 1 in the ERR_STATUS register.

Impact

In a fully functioning system, TEA, MC_TEA and TTL errors are not common occurrences. This limitation should not affect most systems.

Work Around

None.

[ERR2] Disabling port with OUTPUT_EN may cause incorrect packets to be sent

Description

If the following conditions occur concurrently, an end of packet (EOP) control symbol for the packet may not be sent to the physical layer:

- A port is disabled on the Tsi578 by clearing the port's OUTPUT_EN bit in the Serial Port Control CSR
- The port's output buffer receives the last datum of a packet from the ISF
- The physical layer is transmitting the packet to the link partner

This causes the physical layer to send contiguous status controls symbols until the next maintenance packet is sent to the output buffer. Receiving a maintenance packet causes a packet not accepted (PNA) control symbol to be sent. The link then performs error recovery.

Impact

When the Tsi578 is in this state, it cannot send the clock compensation pattern required by the *RapidIO Interconnect Specification (Revision 1.3)*.

Work Around

In order to avoid experiencing this erratum, change all routing tables to discard packets sent to the port about to be disabled before clearing the OUTPUT_EN bit. To recover from this event, reset the port.

[ERR3] Exceeding error threshold limit

Description

When the number of link errors exceeds the threshold and the STOP_FAIL_EN and DROP_EN bits are set to 1 in the SPx_CTL register, the packets currently in the Outbound buffer should be dropped and no further packets are sent. In the Tsi578, however, the queued packets are dropped but subsequent packets are sent. The Tsi578 starts to queue packets after the initial packets are dropped. This behavior does not conform to the *RapidIO Error Management Extensions Specification (Part 8) Revision 1.3.*

Impact

This issue may lead to system congestion.

Work Around

In order to recover from this event, stop traffic flow to the port and reset the port using the SOFT_RST_X1 or SOFT_RST_X4 fields in RapidIO Serial MAC x Digital Loopback and Clock Selection Register (as applicable).

[ERR4] Switch Time-to-Live not supported

Description

The Tsi578 does not support Time-to-Live (TTL) functionality required for a switch in the *RapidIO Interconnect Specification (Revision 1.3), RapidIO Error Management Extensions.*

Work Around

None.

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