Tsi721™ Device Errata

Formal Status

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About this Document

This document discusses device errata for the Tsi721.

Revision History

October 2, 2012, Formal Status

- Updated the status of all existing errata
- Updated the second work around for RapidIO 5 Gbaud initialization failure
- Added new errata:
  - PCIe cannot train in 1x mode with lanes reversed
  - Incorrect operation of PCIe dynamic link width reconfiguration capability
  - PCIe L0s support non-compliant
  - PCIe may not train at 5 Gbaud

September 30, 2011, Preliminary Status

Added BDMA response timeouts cause a resource leak.

July 29, 2011, Preliminary Status

Updated the work around for RapidIO 5 Gbaud initialization failure.

July 6, 2011, Preliminary Status

First release of the *Tsi721 Device Errata*.

Device Errata

Errata	Applicability		Status[a]
	A0 Revision (Tsi721)	A1 Revision (Tsi721A1)	
RapidIO Response Timeout Register is non-compliant	●	●	Viable work around
No RapidIO response size checking	●	●	No plans to fix
RapidIO line loopback does not support arbitrary data	●		Fixed
PCIe MSIXTBL and MSIXPBA incorrect default values	●		Fixed
RapidIO 5 Gbaud initialization failure	●	●	Viable work around
PCIe endpoint does not advertise infinite credits	●	●	No plans to fix
PCIe endpoint handles atomic requests as malformed TLPs	●	●	Viable work around
PCIe endpoint PCIELCAP[MAXLNKSPD] does not limit link speed	●	●	Viable work around
BDMA response timeouts cause a resource leak	●		Fixed
PCIe cannot train in 1x mode with lanes reversed	●	●	Viable work around
Incorrect operation of PCIe dynamic link width reconfiguration capability	●	●	No plans to fix
PCIe L0s support non-compliant	●	●	Viable work around
PCIe may not train at 5 Gbaud	●	●	Viable work around

a. “Viable work around” indicates a work around that allows customers’ products to reach production status.

RapidIO Response Timeout Register is non-compliant

Description

The RapidIO Response Timeout Register (0x00124) is non-compliant with the *RapidIO Specification (Rev. 2.1)*. The position of the register's RSP_TO field is incorrectly located in bits [8:31] when they should reside in bits [0:24].

Impact

The timeout values captured in 0x00124 will be incorrect if software programs this register as defined in Part 6 of the *RapidIO Specification (Rev. 2.1)*.

Work around

Update software to program the RSP_TO field according to its actual location in the Tsi721.

Status

Viable work around.

No RapidIO response size checking

Description

RapidIO responses with an incorrect amount of data can be received from non-compliant devices, or when the system is not correctly configured to handle response timeouts. The Tsi721 does not check that the amount of data in the response transactions is correct. The PCIe completion is formulated with incorrect and/or incomplete data.

Impact

The originator of the PCIe transaction can receive corrupted and/or incomplete data.

Work around

None.

Status

No plans to fix.

RapidIO line loopback does not support arbitrary data

Description

When line loopback is enabled on the RapidIO port (RIO_PLM_SP_IMP_SPEC_CTL[LLB_EN] = 1), any valid 10b code group that decodes to an illegal control character as defined by the *RapidIO Specification (Rev. 2.1)*, and whose most significant bit is 0, will be corrupted on transmission. Note that 10b characters that are not valid 10b codes, or that violate running disparity, are transmitted correctly.

Impact

Random 10b data cannot be looped back by the RapidIO port.

Work around

None. However, some data patterns such as CJPAT can still be looped back correctly.

Status

Fixed in A1 revision.

PCIe MSIXTBL and MSIXPBA incorrect default values

Description

The MSI-X Table Offset Register (0x0A4) and MSI-X Pending Bit Array Offset Register (0x0A8), have incorrect default values. The correct values for these registers are 0x0002C000 and 0x0002A000, respectively.

Impact

Software will not configure MSI-X interrupt table functionality correctly.

Work around

Modify Tsi721's registers as follows:

1. Set EPCTL[REGUNLOCK] to 1.
2. Write 0x0002C000 to MSIXTBL.
3. Write 0x0002A000 to MSIXPBA.
4. Set EPCTL[REGUNLOCK] to 0.

For PCIe peripheral cards the register modifications should be loaded from an EEPROM on the I2C bus. For processor boards that contain a Tsi721, register modifications can be implemented in the board's firmware (in addition to the EEPROM method).

Status

Fixed in A1 revision.

RapidIO 5 Gbaud initialization failure

Description

When the Tsi721's 5-Gbaud configured RapidIO port attempts to initialize after its link partner goes silent, initialization may be unsuccessful.

Impact

The RapidIO link may be unusable.

Work arounds

Either one of the following work arounds can be implemented:

1. Operate the RapidIO links at a 3.125 Gbaud lane rate or less.
2. To avoid this issue, perform the following register writes in the order indicated after the Tsi721 has been powered up. These writes must also be performed after every fundamental reset of the Tsi721.
   a. 0x4F054 – 0x0000006F
   b. 0x4F454 – 0x0000006F
   c. 0x4F854 – 0x0000006F
   d. 0x4FC54 – 0x0000006F
   e. 0x4F04C – 0x00000000
   f. 0x4F44C – 0x00000000
   g. 0x4F84C – 0x00000000
   h. 0x4FC4C – 0x00000000

   However, if the link speed is *altered* to 3.125 Gbaud or lower then the above work around must be removed by performing the following register writes:
   a. 0x4F054 – 0x0000000F
   b. 0x4F454 – 0x0000000F
   c. 0x4F854 – 0x0000000F
   d. 0x4FC54 – 0x0000000F

Status

Viable work around.

PCIe endpoint does not advertise infinite credits

Description

The *PCI Express Base Specification (Rev. 2.1)* requires an endpoint to advertise infinite completion credits by default. The Tsi721 advertises 127 completion credits.

Impact

None.

Work around

None.

Status

No plans to fix.

PCIe endpoint handles atomic requests as malformed TLPs

Description

The *PCI Express Base Specification (Rev. 2.1)* requires an endpoint to handle transactions that it does not support as Unsupported Requests (UR), and to report them as such. The Tsi721 handles atomic operations as malformed TLPs, and reports them as such.

Impact

Unsupported TLPs are reported as malformed TLPs.

Work around

Design error handling software to support the reporting of malformed TLPs.

Status

Viable work around.

PCIe endpoint PCIELCAP[MAXLNKSPD] does not limit link speed

Description

According to the *PCI Express Base Specification (Rev. 2.1)*, the PCIELCAP[MAXLNKSPD] value can be overridden to limit the PCIe link speed. The Tsi721 does not limit the link speed based on the MAXLNKSPD value.

Impact

Links may train at a higher link speed than desired.

Work around

Use the link partner's PCIELCAP[MAXLNKSPD] value to force the Tsi721 to use 2.5 Gbaud link speeds.

Status

Viable work around.

BDMA response timeouts cause a resource leak

Description

When a response timeout occurs for an NREAD, NWRITE_R, Maintenance Read, or Maintenance Write request that is originated by the BDMA engines, the transaction identifier (TID) associated with the request cannot be reused until the Tsi721 is reset.

Impact

The throughput of the above-mentioned transactions is reduced in proportion to the loss of TIDs. If no TIDs are available, the BDMA will stall and cause a network failure.

Work around

Reset the Tsi721.

Status

Fixed in A1 revision.

PCIe cannot train in 1x mode with lanes reversed

Description

A problem occurs when the Tsi721's PCIe lanes are connected in 1x to a root complex port in a reversed setup as such:

Tsi721	Root Complex
PERP[n]	Lane 3
PERP[n+1]	Lane 2
PERP[n+2]	Lane 1
PERP[n+3]	Lane 0

In this configuration, the Tsi721 does not initiate internal lane swapping and cannot train with the root complex.

Impact

The PCIe link is non-functional.

Work around

The following setting allows the Tsi721 to initiate internal lane swapping for all port width configurations:

- In the PHY Link Configuration 0 Register (offset 0x530), set RDETECT = 0b10.
- In the SerDes Configuration Register (0x510), set P2D = 1 and P1D = 1.

Status

Viable work around.

Incorrect operation of PCIe dynamic link width reconfiguration capability

Description

The Tsi721 advertises to its link partners that it supports the PCIe 2.0 dynamic link width reconfiguration capability. When a link partner down-configures a link (for example, from x4 to x1) the Tsi721 supports this capability. However, if the link partner attempts to up-configure the link (for example, x1 to x4), the Tsi721 does not support this change and will keep the link in the down-configured state, x1.

Impact

Maximum PCIe bandwidth is unobtainable.

Work around

None.

Status

No plans to fix.

PCIe L0s support non-compliant

Description

The Tsi721 fails to remain in the L0s IDLE state when the link partner is sending electrical IDLEs. In addition, the device also fails to remain in the L0s IDLE state until it has packets to send.

Impact

L0s support does not result in the expected power savings.

Work around

None.

Status

As per ECN “ASPM Optionality,” approved August 20, 2009 against the *PCI Express Base Specification (Rev. 2.1)*, ASPM support is optional. In Revision A1 of the Tsi721, the reset value of the ASPMS bit was changed from 1 to 0.

PCIe may not train at 5 Gbaud

Description

The Tsi721 occasionally fails to train at 5.0 Gbaud, and instead, powers up at 2.5 Gbaud. This scenario has been observed on various motherboards.

Impact

Maximum PCIe bandwidth cannot be obtained.

Work around

Force the PCIe link to negotiate to 5 Gbaud by setting the ILSCC bit in the PHY Link Configuration 0 Register (offset 0x530) to 0.

Status

Viable work around.

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