F1440

500MHz to 1000MHz Configurable 50Ω or 100Ω DIFF-In to 50Ω SE-Out Variable Gain Amplifier

The F1440 is a high-linearity variable gain RF amplifier with an integrated digital step attenuator (DSA) designed to operate within the 500MHz to 1000MHz frequency range. Using a single 5V power supply, the F1440 typically provides 42.5dB of gain, 3.2dB of noise figure, 41.5dBm of OIP3, and 30dBm OP1dB at its maximum gain setting.

The F1440 is offered in a 5 × 5 mm, 32-VFQFPN package, with an external input BOM configurable differential 50Ω or 100Ω input and single-ended 50Ω output impedances for ease of integration into the signal path.

Competitive Advantage

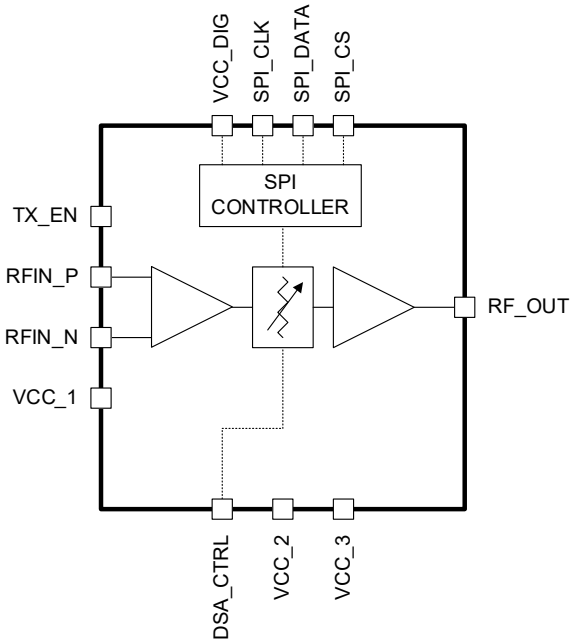
- High level of integration in a compact 5 × 5 mm 32-VFQFPN package
- Uses patented *Glitch-Free™* technologies, providing superior performance and PA damage protection over the entire RF gain range

Applications

- FDD or TDD 5G sub-6GHz wireless infrastructure
- Repeaters and DAS
- General-purpose RF

Features

- Frequency range: 500MHz to 1000MHz
- 42.5dB typical gain at 750MHz
- 3.2dB typical NF at 750MHz
- 41.5dBm typical OIP3 at 750MHz
- 30dBm typical OP1dB at 750MHz
- Configurable 50Ω or 100Ω differential input impedance through external input BOM change
- 31.5dB DSA range with 0.5dB step size
- 5V power supply
- 305mA typical quiescent current consumption
- 1.8V and 3.3V SPI SDI logic compatible
- 1.8V SPI SDO logic compatible
- SPI control for DSA attenuation
- Disable mode for power savings
- Operating temperature (T_{EPAD}) range: -40°C to +105°C
- 5 × 5 mm 32-VFQFPN package



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1. Pin Information

1.1 Pin Assignments

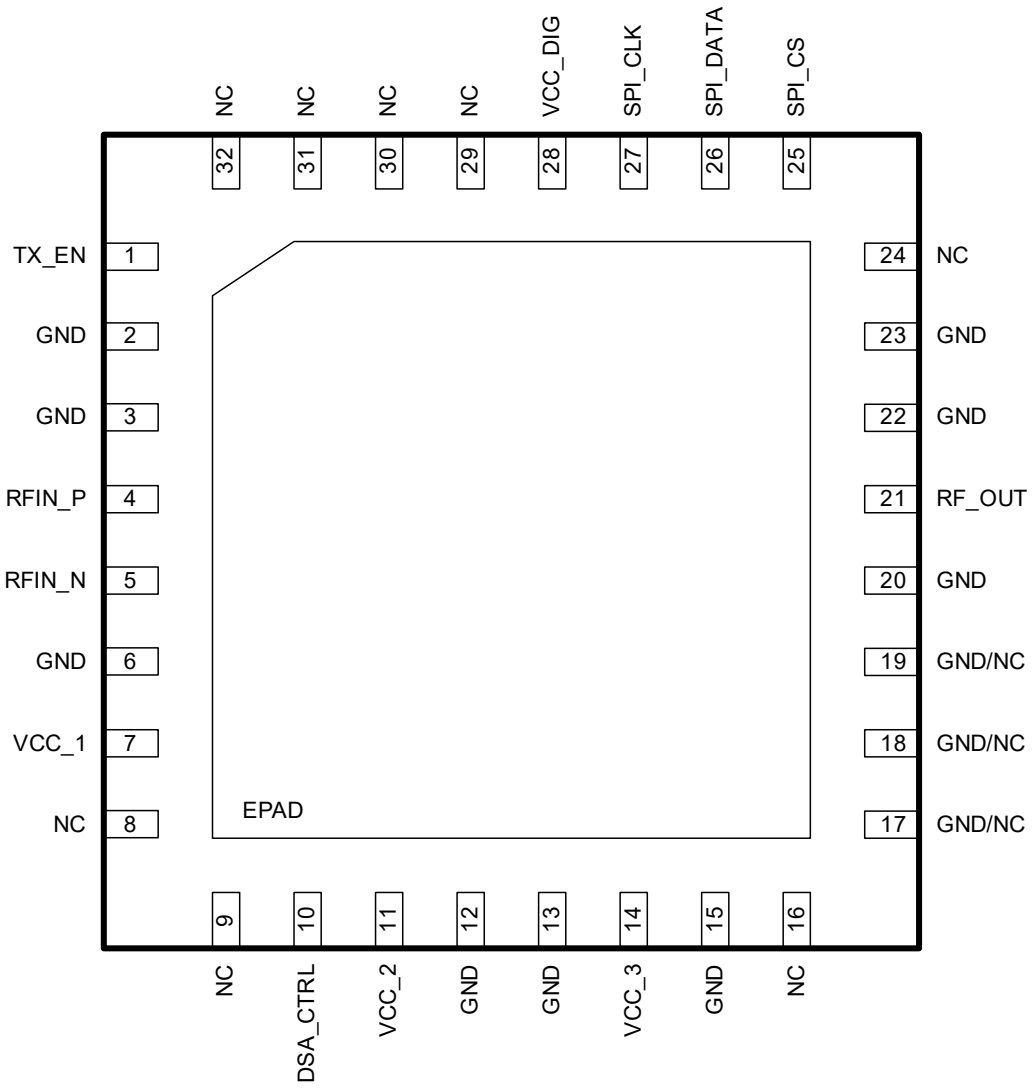


Figure 2. Pin Assignments – Top View

1.2 Pin Descriptions

Number	Name	Description
1	TX_EN	Power-down pin. With logic LOW applied to this pin, the device is powered off. With logic HIGH applied to this pin (or if the pin is left unconnected), the device is in full operation mode. Pin is 1.8V, and 3.3V logic compatible.
2, 3, 6, 12, 13, 15, 20, 22, 23,	GND	Internally grounded. This pin must be grounded with a via as close to the pin as possible.
4	RFIN_P	RF input. Must use an external DC block.
5	RFIN_N	RF input. Must use an external DC block.
7	VCC_1	5V power supply. Use bypass capacitors as close to the pin as possible.

Number	Name	Description
8, 9, 16, 24, 29, 30, 31, 32	NC	No internal connection. Can be left floating or connected to VCC or GND.
10	DSA_CTRL	DSA configuration control pin.
11	VCC_2	5V power supply. Use bypass capacitors as close to the pin as possible.
17, 18, 19	GND/NC	Ground or no connection. These pins can be left unconnected or connected to ground (recommended). If grounded, use a via as close to the pin as possible.
14	VCC_3	5V power supply. Use bypass capacitors as close to the pin as possible.
21	RF_OUT	RF output. Must use an external DC block.
25	SPI_CS	SPI chip-select pin.
26	SPI_DATA	SPI data pin for read and write operations.
27	SPI_CLK	SPI clock pin.
28	VCC_DIG	5V digital power supply. Use bypass capacitors as close to the pin as possible.
-	EPAD	Exposed Pad. Internally connected to ground. Solder this exposed pad to a PCB pad that uses multiple ground vias to provide heat transfer out of the device into the PCB ground planes. These multiple ground vias are also required to achieve the noted RF performance.

2. Specifications

2.1 Absolute Maximum Conditions

Stresses above those listed below can cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods can affect device reliability.

Parameter	Symbol	Minimum	Maximum	Unit
V_{CC} to GND	V_{CC}	-0.3	+5.5	V
SPI_CLK, SPI_DATA, SPI_CS	V_{SPI}	-0.3	V_{CC} + 0.25	V
TX_EN, DSA_CTRL	V_{CTL}	-0.3	V_{CC} + 0.25	V
RFIN Externally Applied DC Current	V_{RFIN}	-1	1	mA
Maximum CW Input Power applied for 24 hours. V_{CC} = 5V, T_{EPAD} = 105°C. 50Ω system. TX_EN = logic HIGH: ON state [1]	$P_{MAX\_IN\_ON}$	-	+6	dBm
Maximum CW Input Power applied for 24 hours. V_{CC} = 5V, T_{EPAD} = 105°C. 50Ω system. TX_EN = logic LOW: OFF state [1]	$P_{MAX\_IN\_OFF}$	-	+6	dBm
Storage Temperature Range	T_{st}	-65	150	°C
Lead Temperature (soldering, 10s)		-	260	°C
Electrostatic Discharge – HBM (JEDEC/ESDA JS-001-2012)	V_{ESDHBM}	-	1000	V
Electrostatic Discharge – CDM (JEDEC 22-C101F)	V_{ESDCDM}	-	500	V

1. Exposure to these maximum RF levels can result in significantly higher I_{CC} current draw because of overdriving the amplifier stages.

2.2 Recommended Operating Conditions

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Unit
Power Supply Voltage	V_{CC}	-	4.75	5	5.25	V
Full Functionality Operating Temperature Range	T_{EPAD1}	Exposed paddle	-40	-	+105	°C
Full Performance Operating Temperature Range	T_{EPAD1}	Exposed paddle	-20	-	+105	°C
Junction Temperature	T_J	SiGe device	-	-	+125	°C
		GaAs device	-	-	+150	°C
RF Frequency Range	f_{RF}	-	500	-	1000	MHz
RFIN Port Impedance	Z_{RFI}	Differential	-	50 or 100	-	Ω
RFOUT Port Impedance	Z_{RFO}	Single-ended	-	50	-	Ω

2.3 Electrical Specifications

2.3.1. General Electrical Specifications

Specifications apply when operated as a TX amplifier with internal tuning optimized for the band (See Register settings listed in section 4.2.2.11), V_{CC} = +5.0V, T_{EPAD} = +25°C, TX_EN = HIGH, Z_S = 100Ω differential, Z_L = 50Ω single-ended, and maximum gain setting. Evaluation Board trace and connector losses are de-embedded, unless otherwise stated.

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Unit
Logic Input High	V_{IH}		***1.17*** [1]	-	3.3	V
Logic Input Low	V_{IL}		-0.3	-	***0.63***	V
SPI Logic Current [2]	I_{SPI}	1.8V	***-100***	-	***100***	µA
		3.3V	***-100***	-	***100***	µA
TX_EN, DSA_CTRL Logic Current	I_{CTL}	1.8V	***-150***	-	***150***	µA
		3.3V	***-150***	-	***150***	µA
Quiescent Current [3]	I_{CC}		-	305	***365***	mA
Standby Current	I_{DD_STBY}	TX_EN pin = LOW	-	4	-	mA
Enable Settling Time [4]	t_{SETTLE_ON}	50% TX_EN control to RF output within 0.25dB and 1° of the on-state final value. T_{EPAD} = -20°C to 105°C, V_{CC} = 4.75V to 5.25V	-	-	1	µs
Disable Settling Time [4]	t_{SETTLE_OFF}	50% TX_EN control to Max gain – 40dB. T_{EPAD} = -20°C to 105°C, V_{CC} = 4.75V to 5.25V	-	-	1	µs
Serial Clock Speed	f_{CLK}		-	-	25	MHz
CS to First Serial Clock Rising Edge	t_{LS}	SPI 3-wire bus. 50% of CS falling edge to 50% of CLK rising edge.	10	-	-	ns
Serial Data Hold Time	t_H	SPI 3-wire bus. 50% of CLK rising edge to 50% of DATA falling edge.	10	-	-	ns
Final Serial Clock Rising Edge to CS	t_{CLS}	SPI 3-wire bus. 50% of CLK rising edge to 50% of CS rising edge.	10	-	-	ns

1. Specifications in the minimum/maximum columns that are shown in ***bold italics*** are confirmed by test. Specifications in these columns that are not shown in bold italics are confirmed by design characterization.
2. Voltage condition refers to SDI logic.
3. I_{CC} refers to the nominal small signal bias current.
4. Speeds are measured after SPI programming is completed (data latched with SPI_CS = HIGH).

2.3.2. 500MHz to 1000MHz Electrical Specifications

Typical specifications apply when operated as a TX amplifier with internal tuning optimized for the band (See Register settings listed in section 4.2.2.11), V_{CC} = +5.0V, T_{EPAD} = +25°C, f_{RF} = 750MHz, TX_EN = HIGH, Z_S = 100Ω differential, Z_L = 50Ω single-ended, and maximum gain setting (DSA = 0dB). Minimum and maximum specifications apply across frequency band, process, recommended operating voltage, and full performance temperature unless otherwise stated.

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Unit
Gain	G		-	42.5	-	dB
		600MHz to 1000MHz	36	-	48	dB
		500MHz to 1000MHz	35.5	-	48	dB
		500MHz to 1000MHz, +105°C	35.5	-	42.5	dB
Gain Slope Relative to Center Frequency	G_{SLOPE}	600MHz to 1000MHz across any ±40MHz BW	-	-	0.8	dB
		500MHz to 1000MHz across any ±40MHz BW	-	-	1.9	dB
		600MHz to 1000MHz across any ±100MHz BW	-	-	1.4	dB
		500MHz to 1000MHz across any ±100MHz BW	-	-	2.8	dB
		600MHz to 1000MHz across any ±200MHz BW	-	-	2.2	dB
		500MHz to 1000MHz across any ±200MHz BW	-	-	2.8	dB
CMRR	CMR		30	-	-	dB
Gain Imbalance	G_{IMB}		-	0.2	-	dB
Phase Imbalance	PH_{IMB}		-	1	-	deg
RF Input Return Loss	RL_{RFIN}		9.5	-	-	dB
RF Output Return Loss	RL_{RFOUT}		8	-	-	dB
Reverse Isolation	ISO_{REV}		-	65	-	dB
Disable Mode Gain	G_{STBY}	STBY = logic LOW, P_{IN} ≤ -15dBm	-	-60	-	dB
DSA Dynamic Range	DSA_{RANGE}		30.5	-	-	dB
DSA Step Size	DSA_{STEP}		0.25	0.5	0.65	dB
DSA Phase Delta	DSA_{PHASE}	Phase change AMIN vs. AMAX	-	10	-	deg
DSA Settling Time	DSA_{SETTLE}	From rising edge of SPI_CS to within 0.1dB of final gain setting, excluding SPI communication	-	-	1	µs

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Unit
DSA Transient Slew Rate	DSA_{SLEW}	For every 0.5 and 1dB attenuation state change combination only.	-	-	75	dB/µs
Noise Figure at -20°C	NF1	DSA = 0dB, 600MHz to 1000MHz	-	-	3.0	dB
		DSA = 0dB, 500MHz to 1000MHz	-	-	3.1	dB
		DSA = 16dB, 600MHz to 1000MHz	-	-	5.2	dB
		DSA = 16dB, 500MHz to 1000MHz	-	-	6.5	dB
Noise Figure at 25°C	NF2	DSA = 0dB	-	3.2	-	dB
		DSA = 16dB	-	5.2	-	dB
Output 3rd Order Intercept Point [1]	OIP3	DSA = 0dB, 600MHz to 1000MHz	37	41.5	-	dBm
		DSA = 0dB, 500MHz to 1000MHz	36	41.5	-	dBm
		DSA = 16dB	33	41.5	-	dBm
		DSA = 31.5dB	20	29.5	-	dBm
Output 1dB Compression Point	OP1dB	DSA = 0dB	25	30	-	dBm
		DSA = 16dB	19	28	-	dBm
		DSA = 31.5dB	4	13	-	dBm
ACLR	ACP	E-TM1.1 at Pout = 10dBm DSA = 0dB	-	-62	-	dBc
Stability K-Factor	K	10MHz to 13.5GHz	1	-	-	

1. Pout = (OP1dB -10dB) total power, Δf = 1MHz - 100MHz.

2.4 Thermal Characteristics

Parameter	Symbol	Value	Unit
Junction to Ambient Thermal Resistance	θ_{JA}	31.45	°C/W
Junction to Case Thermal Resistance. (Case is defined as the exposed paddle)	$\theta_{JC\_BOT\_SIGE}$	5.8	°C/W
	$\theta_{JC\_BOT\_GAAS}$	11.8	°C/W
Moisture Sensitivity Rating (Per J-STD-020)	-	MSL1	-

2.4.1. Elevated Operating Temperature Considerations

This F1440 supports applications in a natural convection environment that does not have any thermal conductivity through ambient air. The printed circuit board (PCB) is typically in a sealed enclosure without any natural or forced air flow and is kept at or below a specific temperature. The device package design incorporates an exposed pad (EPAD) with enhanced thermal parameters, which is soldered to the PCB where most of the heat escapes from the bottom of the exposed pad. For this type of application, it is recommended that the maximum recommended junction temperature is not exceeded when operating above the maximum recommended full functional operating temperature of 105°C to maintain long-term reliability. The junction temperature can be calculated using the following equation:

$T_J = T_{EPAD} + (\theta_{JC\_BOT} \times P_D)$, where

- T_J = Junction temperature at steady state condition in °C.
- T_{EPAD} = Exposed pad temperature at steady state condition in °C.
- θ_{JC_BOT} = Junction to case thermal resistance (case is defined as the exposed paddle) in °C/W.
- P_D = Device power dissipation in W at the desired operating configuration.

The following is an example calculation given an EPAD temperature of 108°C.

Variable	Value
T_{EPAD}	108°C
$\theta_{JC\_BOT\_SIGE}$	5.8°C/W
$\theta_{JC\_BOT\_GAAS}$	11.8°C/W
P_D	2.0W

- T_{J_SIGE} = 108°C + (5.8°C/W x 2.0W) = 119.6°C
- T_{J_GAAS} = 108°C + (11.8°C/W x 2.0W) = 131.6°C

For the variables above, the junction temperature is equal to 119.6°C for the SiGe IC and 131.6°C for the GaAs IC. Since this is below the maximum recommended junction temperature of 125°C for the SiGe IC and 150°C for the GaAs IC, there are no long-term reliability concerns.

3. Typical Operating Conditions

Unless otherwise stated, the typical operating graphs were measured under the following conditions:

- V_{CC} = 5.0V
- TX_EN = HIGH
- T_{EPAD} = +25°C
- f_{RF} = 750MHz
- Z_S = 100Ω differential, Z_L = 50Ω single-ended
- Pout = 0dBm/tone and 10MHz tone spacing for OIP3

3.1 Typical Performance Curves

Note: 100Ω BOM (maximum gain condition unless otherwise stated)

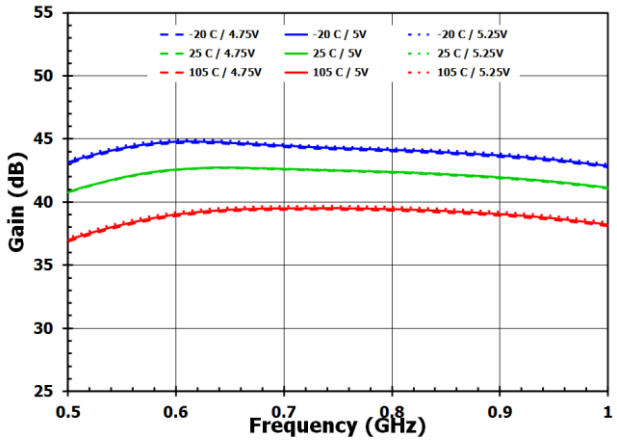


Figure 3. Gain

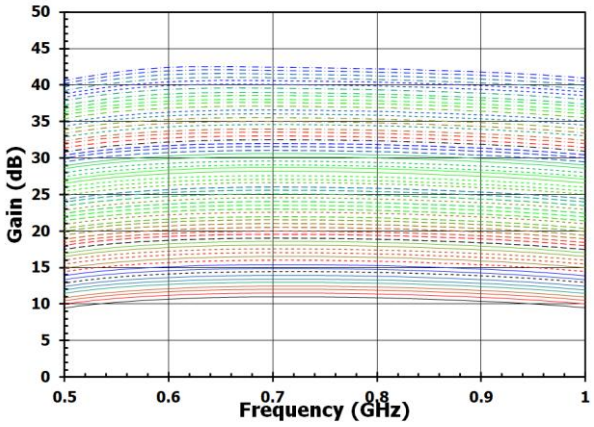


Figure 4. Gain vs. Attenuation State, 5V, 25°C

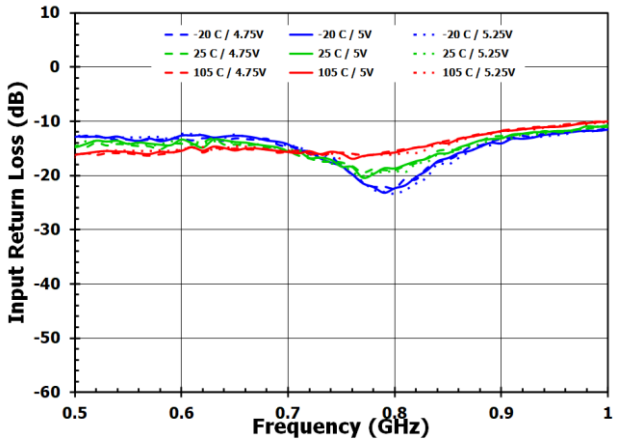


Figure 5. Input Return Loss

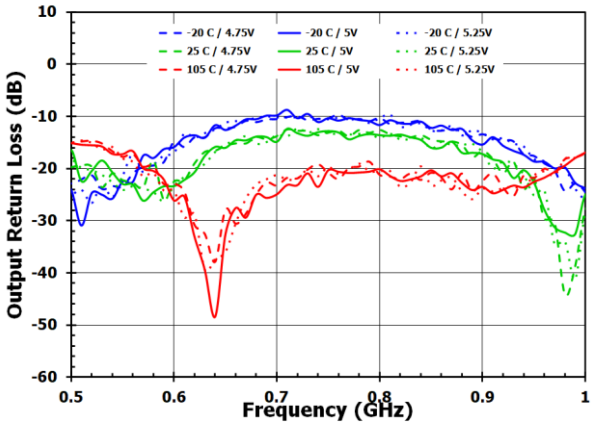


Figure 6. Output Return Loss

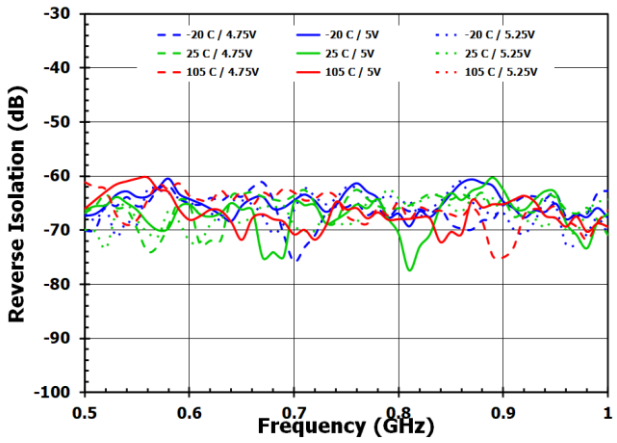


Figure 7. Reverse Isolation

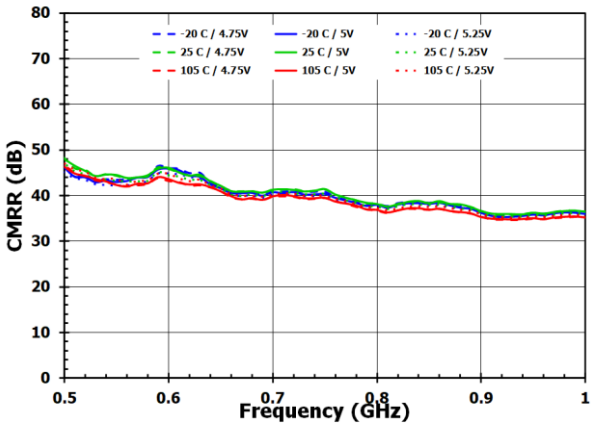


Figure 8. CMRR

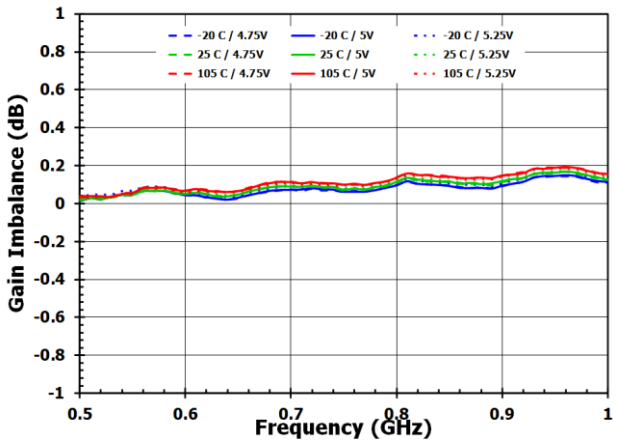


Figure 9. Gain Imbalance

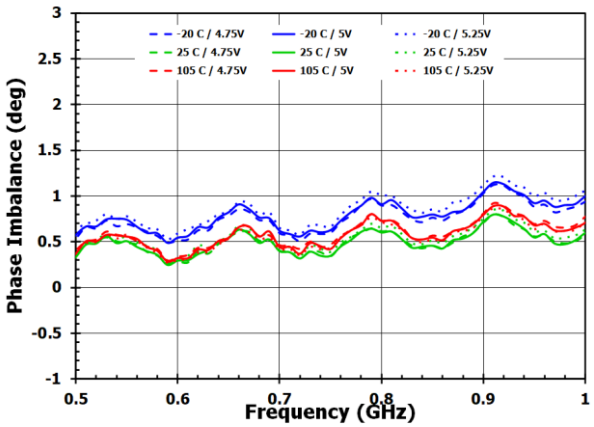


Figure 10. Phase Imbalance

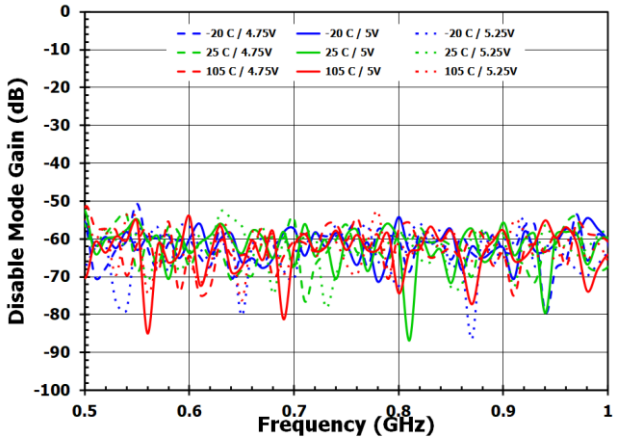


Figure 11. Disable Mode Gain

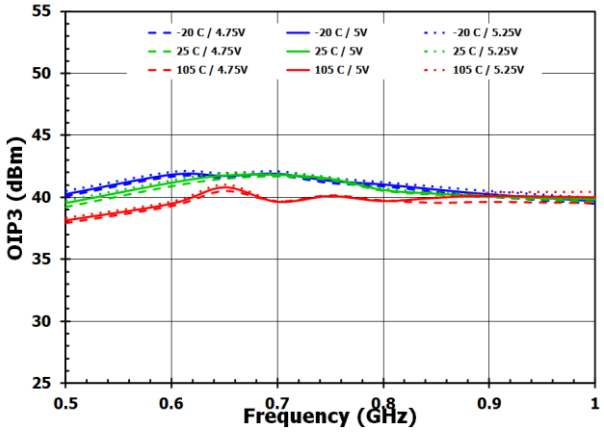


Figure 12. OIP3, DSA = 0dB, 100MHz Tone Spacing

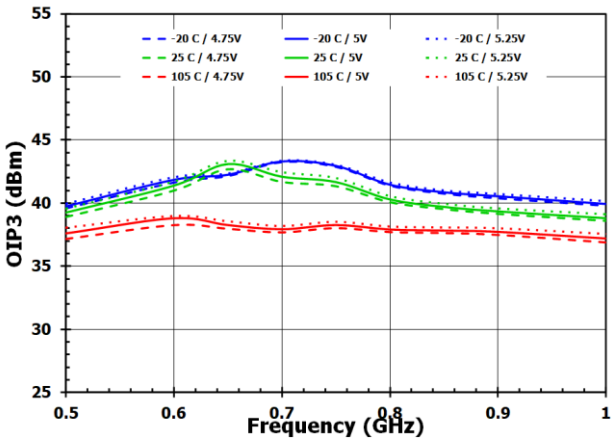


Figure 13. OIP3, DSA = 16dB, 100MHz Tone Spacing

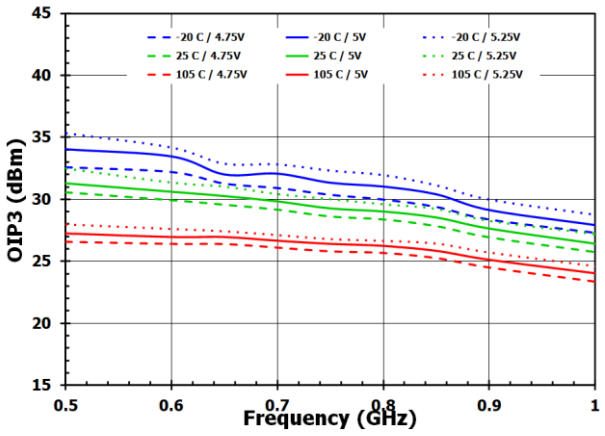


Figure 14. OIP3, DSA = 31.5dB, 100MHz Tone Spacing

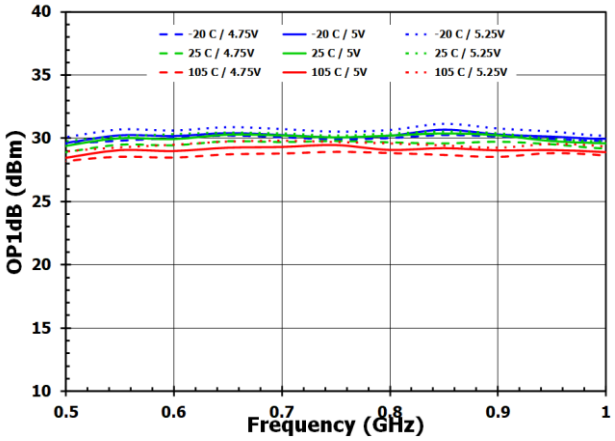


Figure 15. OP1dB, DSA = 0dB

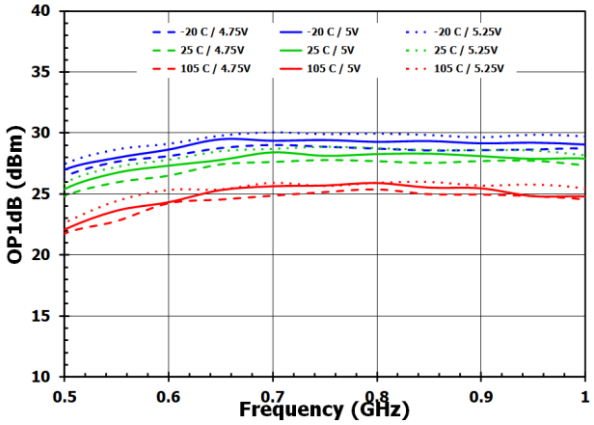


Figure 16. OP1dB, DSA = 16dB

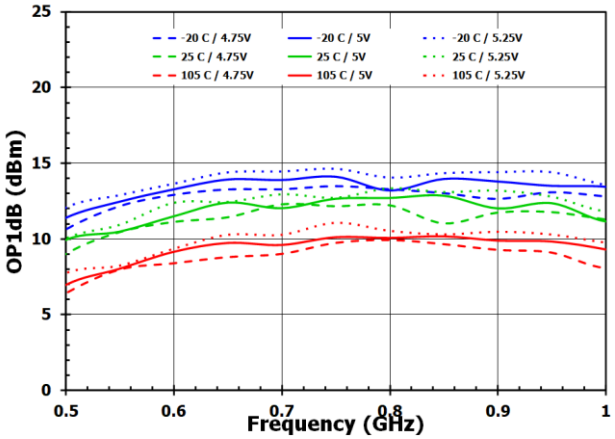


Figure 17. OP1dB, DSA = 31.5dB

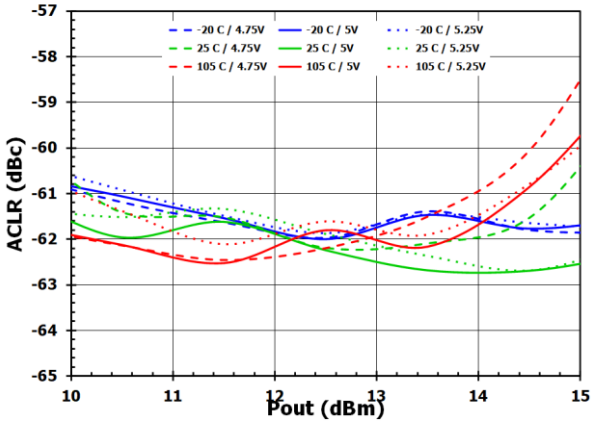


Figure 18. ACLR, DSA = 0, at 750MHz

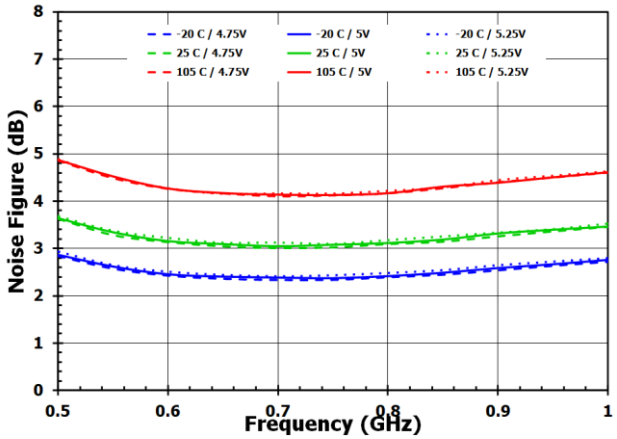


Figure 19. Noise Figure, DSA = 0dB

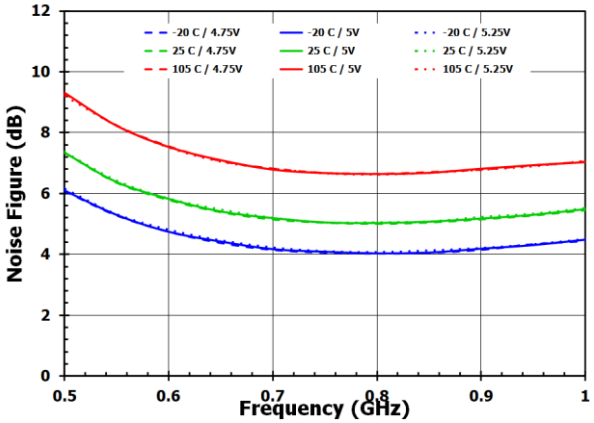


Figure 20. Noise Figure, DSA = 16dB

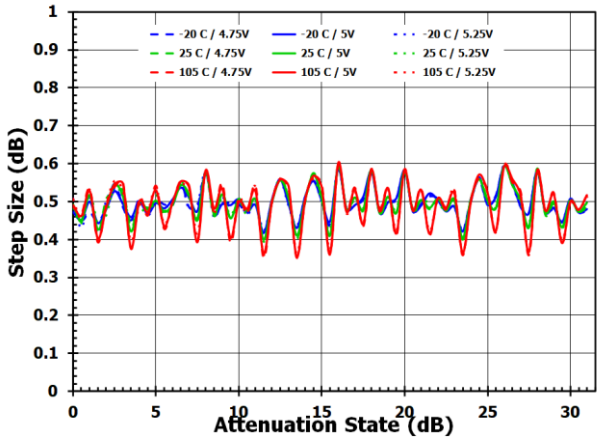


Figure 21. DSA Step Size at 750MHz

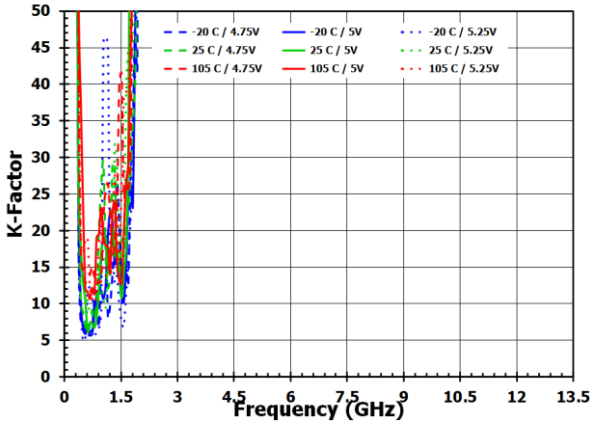


Figure 22. K-Factor

4. Functional Description

4.1 TX Enable

The F1440 can be disabled for low current consumption by applying a logic voltage to the TX_EN (pin 1) using Table 1.

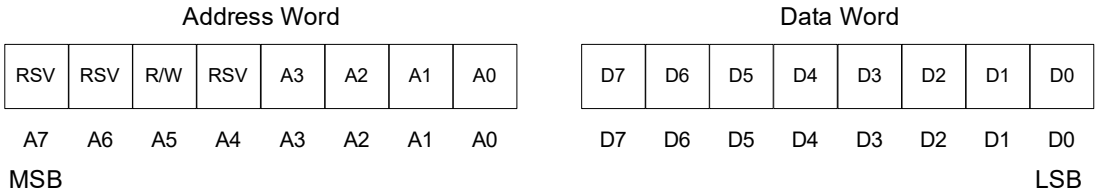
Table 1. TX Enable Truth Table

TX_EN	Condition
Logic HIGH / NC	Full operation, amplifiers ON
Logic LOW	Amplifiers OFF, DSA set to maximum attenuation

4.2 Serial Programming

4.2.1. SPI Protocol

The F1440 includes an SPI interface that is used primarily to program the device's on-chip digital step attenuator and bias tuning functions. The SPI protocol uses an 8-bit address word followed by an 8-bit data word. The SPI bus consists of three wire signals: Serial Clock (SPI_CLK), Chip Select Bit (SPI_CS), and Serial Data (SPI_DATA). The SPI_DATA line is bi-directional mode and is used for READ and WRITE operations as defined by bit A5 in the Address word.



4.2.2. Device Register Map

4.2.2.1. Address Word Bit Definition

Bits	Name	Description
7:6	RSV	Reserved bits. Do not care values.
5	R/W	Defines Read or Write mode. 0 = Read 1 = Write
4	RSV	Reserved bits. Do not care values.
3:0	REG_ADD	Register Address to Read or Write.

4.2.2.2. Attenuation Setting Register (DSA_SET)

The DSA_SET register sets the device attenuation setting when the DSA_CTRL pin is logic LOW.

Address: 0

Bits	Name	Type	Default	Description
7:0	ATT1	R/W	0x0	8-bit attenuation setting (MSB is bit 7).

4.2.2.3. DSA_CTRL Enabled Attenuation Setting Register (DSA_CTRL_SET)

The DSA_CTRL_SET register sets the device attenuation setting when the DSA_CTRL pin is logic HIGH.

Address: 1

Bits	Name	Type	Default	Description
7:0	ATT2	R/W	0x0	8-bit attenuation setting (MSB is bit 7).

4.2.2.4. Bias Control Register (BIAS_CTRL_SET)

Address: 2

Bits	Name	Type	Default	Description
7:0	RSV	R/W	0x0	Reserved for factory use only.

4.2.2.5. Common Controls Register (COM_CTRL_SET)

Address: 3

Bits	Name	Type	Default	Description
7:6	RSV	R/W	0x0	Reserved for factory use only.
5:3	BG_SET	R/W	0x0	Bandgap current reference setting.
2:0	PTAT_SET	R/W	0x0	PTAT current reference setting.

4.2.2.6. Driver Register - 1 (DRV1_SET)

Address: 4

Bits	Name	Type	Default	Description
7	RSV	R/W	0x0	Reserved for factory use only.
6	DRV_PTBG	R/W	0x0	Driver bias profile selection: 0 = Bandgap 1 = PTAT
5:3	RSV	R/W	0x0	Reserved for factory use only.
2:0	DRV_BIAS	R/W	0x0	Driver bias control.

4.2.2.7. Driver Register - 2 (DRV2_SET)

Address: 5

Bits	Name	Type	Default	Description
7:0	RSV	R/W	0x0	Reserved for factory use only.

4.2.2.8. Driver Register – 3 (DRV3_SET)

Address: 6

Bits	Name	Type	Default	Description
7	RSV	R/W	0x0	Reserved for factory use only.
6:5	DRV_FEED_CAP	R/W	0x0	Driver feedback cap control.
4:0	RSV	R/W	0x0	Reserved for factory use only.

4.2.2.9. Stage-1 Register (STG1_SET)

Address: 7

Bits	Name	Type	Default	Description
7:0	RSV	R/W	0x0	Reserved for factory use only.

4.2.2.10. Chip ID Register (CHIPID_SET)

Address: 8

Bits	Name	Type	Default	Description
7:6	MFR_ID	R	0x2	Renesas manufacturer ID code.
5:4	PRO_ID	R	0x0	Renesas product ID code.
3:0	DEVICE_ID	R	0x1	Renesas device ID code.

4.2.2.11. Control and Configuration Registers

Register Addresses 2 to 7 are used for device configuration as determined through factory test. The default values listed should be used and loaded after device start-up to ensure performance as shown in the datasheet.

Bits	Register Address	Type	Default	Description
7:0	2	R/W	0xA8	Control Register.
7:0	3	R/W	0x14	Common Controls Register.
7:0	4	R/W	0x9F	Driver Register 1.
7:0	5	R/W	0xFA	Driver Register 2.
7:0	6	R/W	0x1F	Driver Register 3.
7:0	7	R/W	0x0	Stage 1 Register.
7:0	8	R	0x81	Chip ID Register.

4.2.3. DSA Truth Tables

For optimized DSA step size performance, a unique set of DSA settings are recommended for specific frequency ranges of operation.

Att (dB)	0.5 – 1.0GHz	
	DEC	BIN
0 (Max Gain)	127	01111111
0.5	126	01111110
1	125	01111101
1.5	124	01111100
2	187	10111011
2.5	186	10111010
3	121	01111001
3.5	120	01111000
4	119	01110111
4.5	118	01110110
5	117	01110101
5.5	116	01110100
6	179	10110011
6.5	178	10110010
7	113	01110001
7.5	112	01110000
8	175	10101111
8.5	110	01101110
9	109	01101101
9.5	108	01101100
10	107	01101011
10.5	106	01101010
11	105	01101001
11.5	104	01101000
12	39	00100111
12.5	38	00100110
13	165	10100101
13.5	164	10100100
14	35	00100011
14.5	34	00100010
15	161	10100001

Att (dB)	0.5 – 1.0GHz	
	DEC	BIN
15.5	160	10100000
16	159	10011111
16.5	94	01011110
17	93	01011101
17.5	92	01011100
18	155	10011011
18.5	90	01011010
19	89	01011001
19.5	88	01011000
20	151	10010111
20.5	86	01010110
21	85	01010101
21.5	84	01010100
22	83	01010011
22.5	82	01010010
23	81	01010001
23.5	80	01010000
24	15	00001111
24.5	14	00001110
25	141	10001101
25.5	140	10001100
26	11	00001011
26.5	138	10001010
27	73	01001001
27.5	72	01001000
28	135	10000111
28.5	70	01000110
29	69	01000101
29.5	68	01000100
30	3	00000011
30.5	2	00000010
31	1	00000001
31.5	0	00000000

4.2.4. Timing Diagrams

4.2.4.1. Register Write

A register write sequence is started by asserting the SPI_CS pin to logic 0 and ends by de-asserting the SPI_CS pin to logic 1. A register write is recognized by setting the Address word bit 5 to a logic 1. Data should be clocked in MSB first.

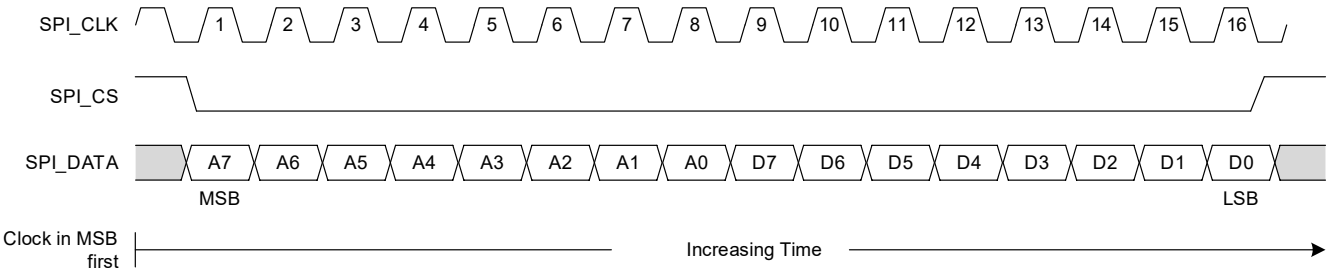


Figure 23. Write Mode Timing Diagram

4.2.4.2. Register Read

A register read sequence is started by asserting the SPI_CS pin to logic 0 and ends by de-asserting the SPI_CS pin to logic 1. A register read is recognized by setting the Address word bit 5 to a logic 0. Data should be clocked in MSB first. On a read access, data is clocked out on the next clock cycle after the last Address bit is clocked in. Note that the data output can be delayed as long as there is no SPI_CLK signal while SPI_CS is a logic 0. Data output will resume on the next active clock cycle.

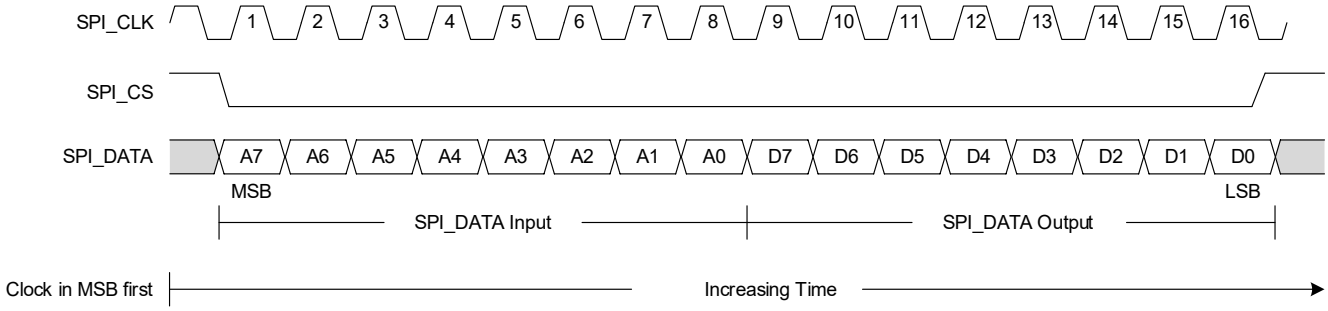


Figure 24. Read Mode Timing Diagram

4.2.4.3. SPI Timing Information

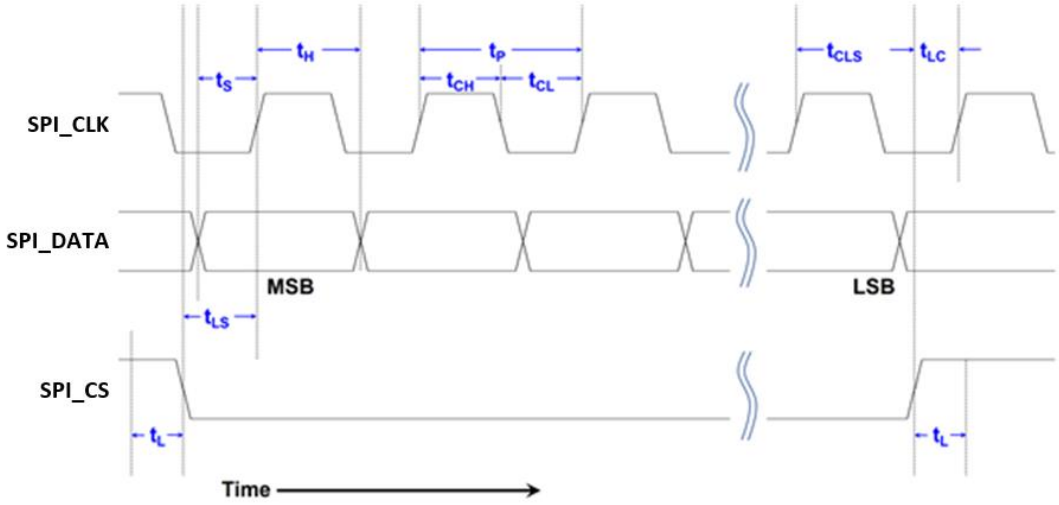


Figure 25. SPI Timing Information

Table 2. Digital Specification

Parameter	Symbol	Minimum	Maximum	Unit
CLK Frequency	f_C	-	25	MHz
CLK High Duration Time	t_{CH}	20	-	ns
CLK Low Duration Time	t_{CL}	20	-	ns
CLK Period [1]	t_P	40	-	ns
DATA to CLK Setup Time	t_S	10	-	ns
CLK to DATA Hold Time	t_H	10	-	ns
Final CLK Rising Edge to SPI_CS Rising Edge	t_{CLS}	10	-	ns
SPI_CS to CLK Setup Time	t_{LS}	10	-	ns
SPI_CS Trigger Pulse Width	t_L	10	-	ns
SPI_CS Trigger to CLK Setup Time [2]	t_{LC}	10	-	ns

1. $(t_{CH} + t_{CL}) \geq 1/f_C$.
2. Once all desired DATA is clocked in, t_{LC} represents the time SPI_CS high needs to occur before any subsequent CLK signals.

4.2.5. DSA Mode Control

The DSA_CTRL pin sets the DSA setting to a pre-programmed value by applying a logic voltage to pin 10 as defined by Table 3. The default programmed attenuation setting is 31.5dB and can be updated through an SPI command. The programmed attenuation setting is reset back to the default value when power to the device is reset.

Table 3. DSA_CTRL Truth Table

DSA_CTRL	Condition
Logic HIGH	DSA set to pre-programmed value
Logic LOW / NC	DSA setting controlled by SPI command

5. Evaluation Board (EVB) Information

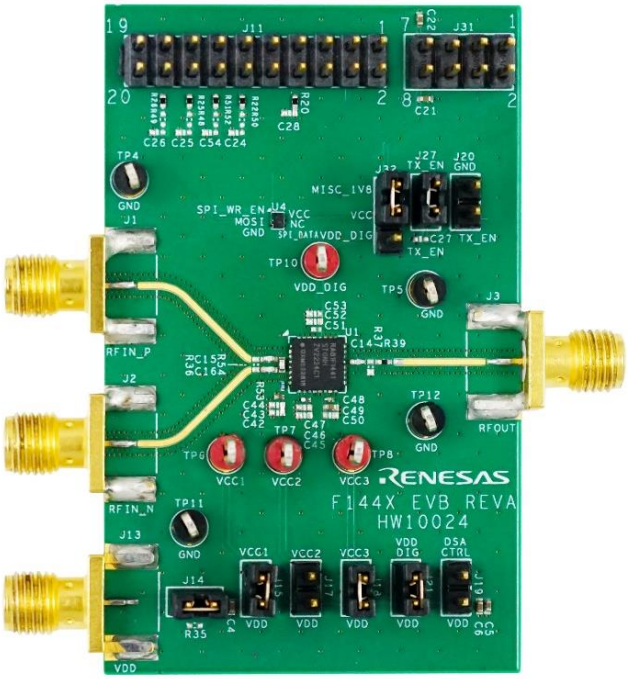


Figure 26. Evaluation Board – Front

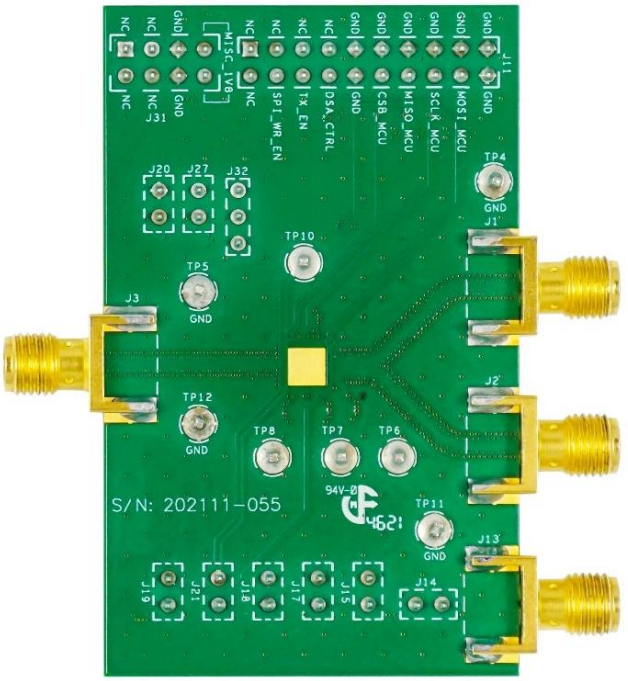


Figure 27. Evaluation Board – Back

5.1 Evaluation Board Schematic

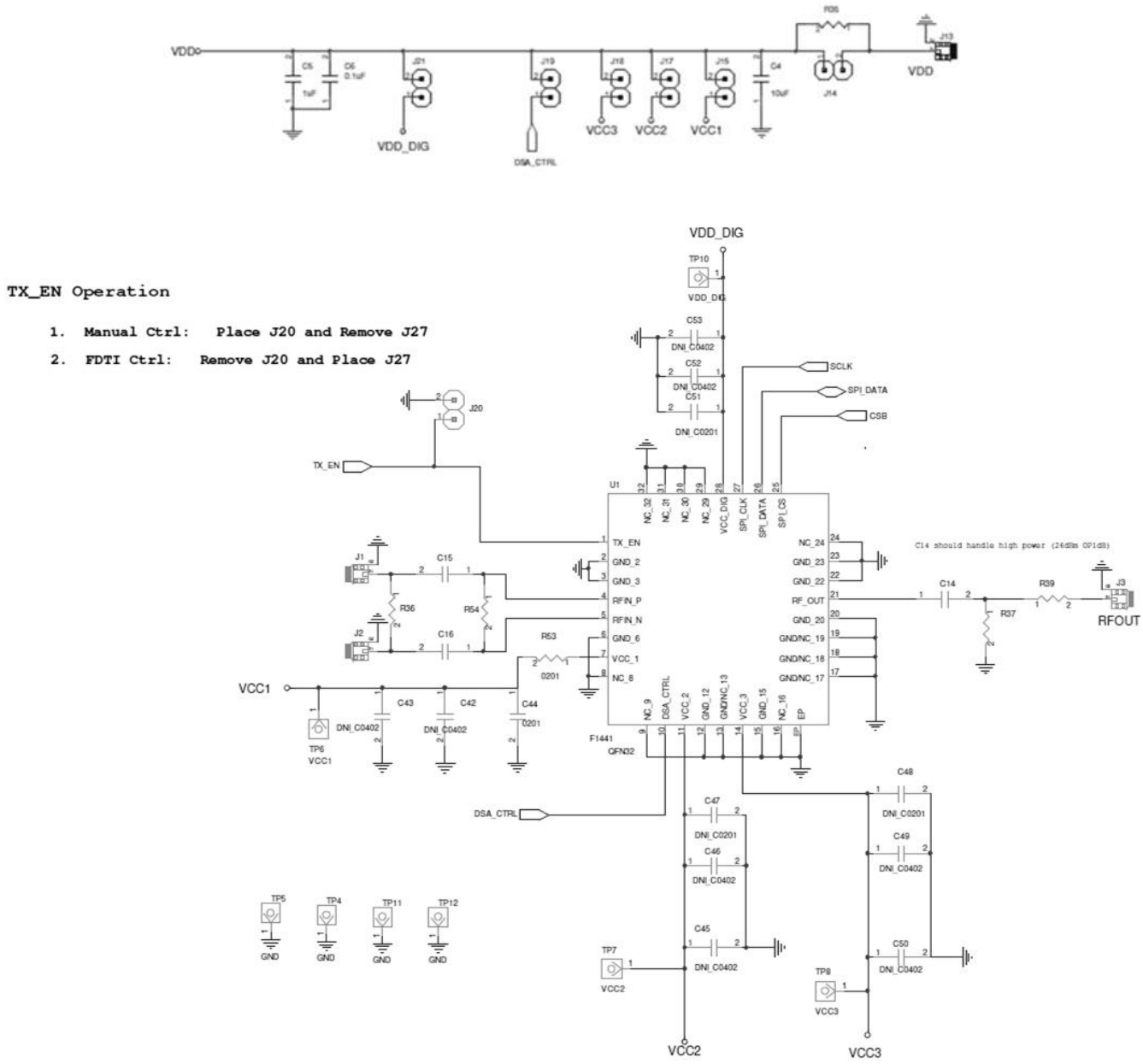


Figure 28. Evaluation Board Circuit Schematic – Image 1

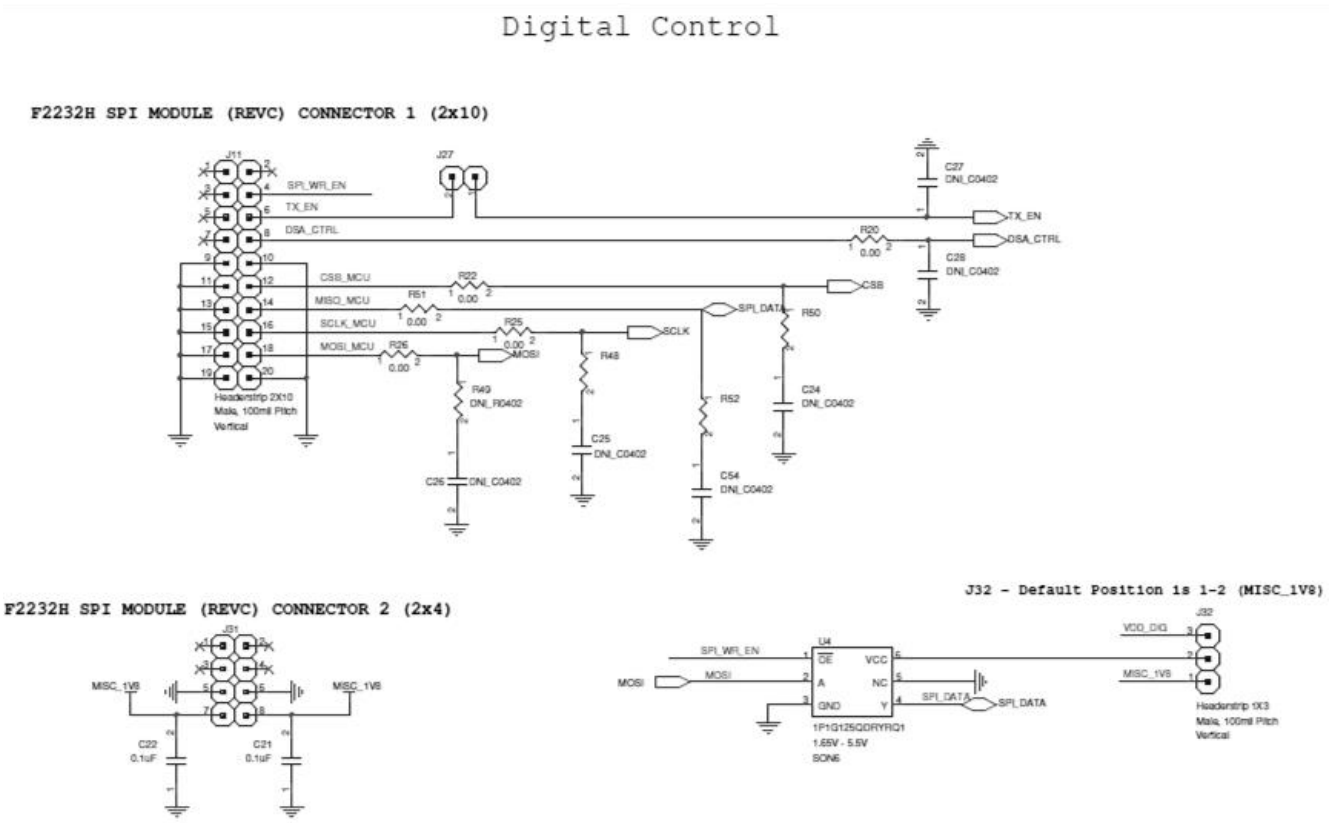


Figure 29. Evaluation Board Circuit Schematic – Image 2

5.2 Evaluation Kit (EVK) Information

For instructions on how to use the EVB and graphical user interface software, see the *F1440 EVK Manual.*

5.3 Bill of Materials

Table 4. Evaluation Board Bill of Material (BOM)

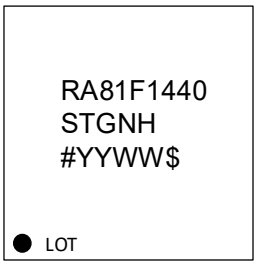
Part Reference	Qty	Description	Manufacturer Part #	Manufacturer
C4	1	10uF ± 20%, 6.3V, X5R Surface Mount Capacitor (0402)	GRM155R60J106M	Murata Electronics
C5	1	1uF ± 10%, 25V, X5R Surface Mount Capacitor (0402)	GRM155R61A105KE15D	Murata Electronics
C6,C21,C22	3	0.1uF ± 10%, 50V, X5R Surface Mount Capacitor (0402)	GRM155R61H104K	Murata Electronics
C14	1	1nF ± 0.05%, 25V, X5R Surface Mount Capacitor (0402)	GRM1555C1H102JA01D	Murata Electronics
C15,C16	2	4.7nH ± 0.1nH, 750mA, Surface Mount Inductor (0402)	LQW15AN4N7B00	Murata Electronics
C48	1	10nF ± 10%, 25V, X5R Surface Mount Capacitor (0201)	GRM033R71E103KE14	Murata Electronics
C49	1	100pF ± 5%, 50V, X5R Surface Mount Capacitor (0402)	GRM1555C1H101JA01D	Murata Electronics
C44	1	1uF ± 20%, 10V, X5R Surface Mount Capacitor (0201)	GRM033C81A105ME05D	Murata Electronics
C47	1	100pF ± 5%, 100V, X5R Surface Mount Capacitor (0201)	GRM0335C1H101JA01J	Murata Electronics
C24,C25,C26,C27,C28,C42,C43,C45,C46,C50,C52,C53,C54	-	DNI_C0402	-	-

Part Reference	Qty	Description	Manufacturer Part #	Manufacturer
C51	-	DNI_0201	-	-
J1,J2,J3,J13	/4	Cinch: SMA JACK STR 50 OHM EDGE MNT, Fits 0.062" board	142-0701-851	Cinch
J11	1	Molex: Header Dual, Gold, Unshrouded, Breakaway, 100mil pitch, 0.240 inch contact mating length	10-89-7200	Molex
J14,J15,J17,J18,J19, J20,J21,J27	8	Molex: Header, Gold, Unshrouded, Breakaway, 100mil pitch, 0.240 inch contact mating length	22-28-4023	Molex
J31	1	Molex: C-Grid Header Dual, Gold, Unshrouded, Breakaway, 100mil pitch	10-89-7080	Molex
J32	1	Molex: Header, Gold, Unshrouded, Breakaway, 100mil pitch, 0.240 inch contact mating length	22-28-4033	Molex
R20,R22,R25,R26, R39,R51	6	0Ω 1/10W Surface Mount Resistor (0402)	ERJ-2GE0R00	Panasonic
R54	1	4pF ± 0.1pF, 50V, Surface Mount Capacitor (0402)	GJM0335C1H4R0BB01	Murata Electronics
R35,R37,R48,R49, R50,R52	6	DNI_R0402	-	-
R36	1	1.5pF ± 0.1pF, 50V, Surface Mount Capacitor (0201)	GJM0335C1H1R5BB01	Murata Electronics
R53	1	15nH ±0.3%, 300mA, Surface Mount Inductor (0201)	LQP03HQ15NH02	Murata Electronics
TP4,TP5,TP11,TP12	4	Keystone Electronics: Phosphor Bronze Wire Loop, heat resistant nylon base	5006	Keystone
TP6	1	Keystone Electronics: Phosphor Bronze Wire Loop, heat resistant nylon base	5010	Keystone
TP7	1	Keystone Electronics: Phosphor Bronze Wire Loop, heat resistant nylon base	5010	Keystone
TP8	1	Keystone Electronics: Phosphor Bronze Wire Loop, heat resistant nylon base	5010	Keystone
TP10	1	Keystone Electronics: Phosphor Bronze Wire Loop, heat resistant nylon base	5010	Keystone
U1	1	Renesas:500MHz – 1000MHz Configurable 50Ω or 100Ω DIFF-In to 50Ω SE-Out Variable Gain Amplifier 5 × 5 mm 32-VFQFPN package	F1440	Renesas
U4	1	TI: Buffer, Non-Inverting 1 Element 1 Bit per Element 3-State Output 6-SON (1.45x1)	1P1G125QDRYRQ1	Texas Instruments

6. Package Outline Drawings

The package outline drawings are located at the end of this document and are accessible from the Renesas website (see package links in Ordering Information). The package information is the most current data available and is subject to change without revision of this document.

7. Marking Diagram

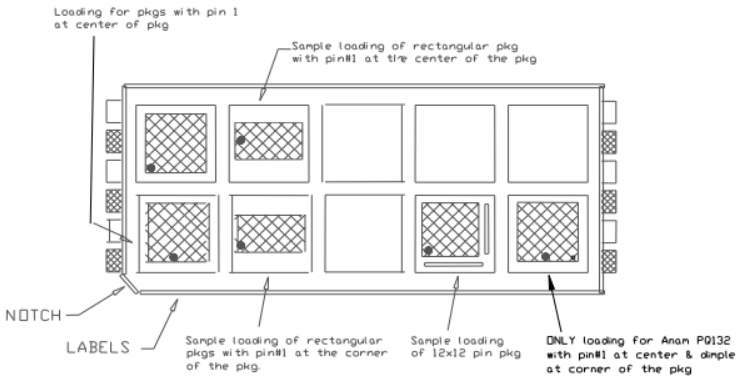
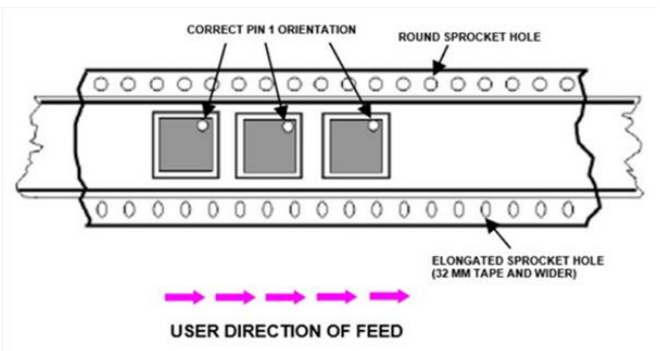


- Lines 1 and 2: truncated part number.
- Line 3: “#” denotes the stepping number; “YYWW” indicates two digits for the year and two digits for the work week that the part was assembled; “$” denotes the assembly site.
- “LOT” denotes the lot number.

8. Ordering Information

Part Number	Package	MSL Rating	Carrier Type	Temperature Range
RA81F1440STGNH#BB0	5.0 × 5.0 mm 32-VFQFPN	MSL1	Tray	-40°C to +105°C
RA81F1440STGNH#KB0	5.0 × 5.0mm 32-VFQFPN	MSL1	Reel	-40°C to +105°C
RTKA81F1440ST000RU	Evaluation Kit (EVK)			

Table 5. Pin 1 Orientation in Tray and Reel Packaging

Part Number Suffix	Pin 1 Orientation	Illustration
BBO (Tray)	See illustration	
KB0 (Reel)	Quadrant 2 (EIA-481-E)	

9. Revision History

Revision	Date	Description
1.05	Aug 15, 2024	▪ Changed Evaluation Kit description for RTKA81F1440ST000RU to EVK from EVB in Ordering Information. ▪ Updated Tray (BBO) orientation diagram in Table 5.
1.04	Mar 1, 2024	Updated table footnote in section 2.3.2.
1.03	Jan 9, 2024	Corrected register address 8 default value to 0x81 from 0x51 in section 4.2.2.11.
1.02	Sep 7, 2023	▪ Replaced the use of the term “Evaluation Kit (EVK)” with “Evaluation Board (EVB)”. ▪ Replaced the use of the term “Evaluation System (EVS)” with “Evaluation Kit (EVK)”.
1.01	Mar 31, 2023	▪ Added maximum values to gain specifications. ▪ Implemented minor formatting changes.
1.00	Jan 19, 2023	Initial release.